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EDN

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEER S

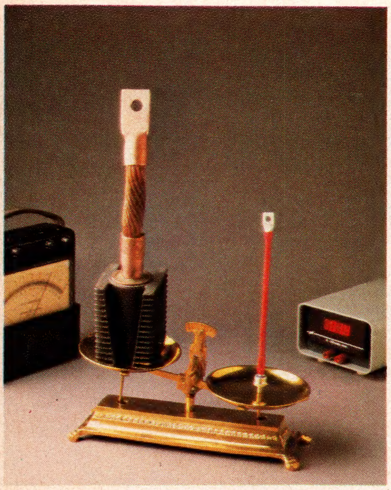
Modern rectifiers tip the scales in your design's favor

0-50,000 IN 0.7 NSEC.

INTRODUCING OUR 1986 COMPACTS.

Volume 31, Number 2 EDN January 23, 1986

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Modern, compact rectifiers outweigh their bulky predecessors when it comes to delivering high currents, low leakage, and improved efficiency. See pg 126. (Photo courtesy International Rectifier)*

DESIGN FEATURES

Continued on page 7

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8840A	$760	8842A	$995
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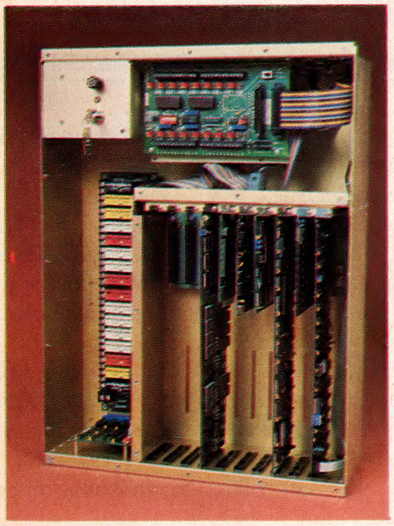
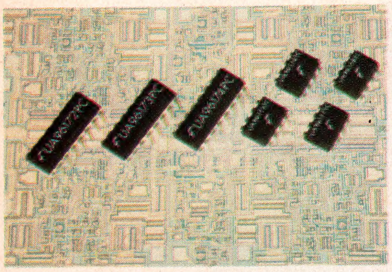
CIRCLE NO 10

Continued from page 5



***Ruggedized IBM PC-compatible computers** can prove cost effective in industrial applications; such hardware is less expensive than minicomputer hardware, and system development time can be relatively short (pg 79).*



***Whether you plan to implement** RS-232C communications links or ones based on RS-422 or -485 specs, you'll find a variety of chips that can simplify your design tasks (pg 93).*

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

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HEWLETT PACKARD

CIRCLE NO 11

DS-15528

Continued from page 7

EDN

January 23, 1986

EDITORIAL

The hottest developments in local-area networks are taking place in factories, not offices. Once again, electronics suppliers are discovering that they must supply what the marketplace wants, not what they think it needs.

NEW PRODUCTS

PROFESSIONAL ISSUES

LOOKING AHEAD

Growth in LAN use is key to improved plant productivity. . .Color-graphics CRTs gain on monochrome, but slowly.

DEPARTMENTS

BPA ABP

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National Semiconductor Corporation

Finally, a logic analyzer and a dual-channel scope

Quickly unravel tough digital/ new two-in-one powerhouse

The new HP 1631A/D Logic Analyzer is the first commercially available instrument to combine a full-featured logic analyzer with an advanced 200 Megasample/second dual-channel general purpose digitizing oscilloscope — both in the same functional package. Now the logic designer's two most important diagnostic tools are available simultaneously, allowing sophisticated cross-domain (logic vs. analog) analysis. Capture analog waveforms based on digital states or timing relationships and then view both logic patterns and analog signals simultaneously on the same screen. Absolute time correlation between logic and scope traces lets you analyze timing patterns based on an analog event. The result is a powerhouse combination of instrument capability and price/performance that far surpasses any previously available solution, plus it's HP-IB programmable.

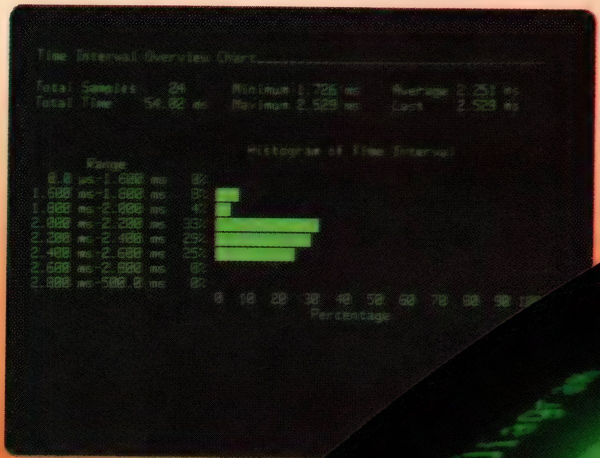
Logic analysis in the HP tradition.

The HP 1631A/D gives you complete logic analysis in today's 16-bit environments. Its 100 MHz timing analyzer section gives you up to 16 channels of simultaneous acquisition. You can set the HP 1631A/D to capture single shot, cumulative mode, or even continue acquisition until your special conditions are met, for fully automatic "babysitting". Extensive pattern triggering and trigger qualification capabilities further extend your diagnostic horizons. The HP 1631A/D also includes a wide array of real-time processing and post-processing options such as mean and standard, min/max, state indexing and storage, and software performance analysis histograms.

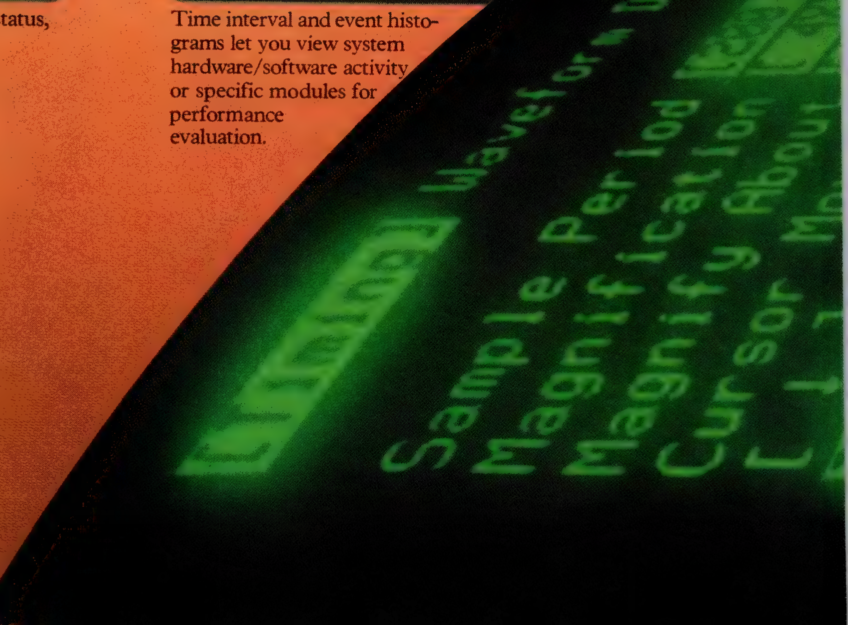
A 200 Megasample/second scope for powerful cross-domain analysis.

Impressive as the HP 1631A/D's logic analysis credentials are, you begin to feel its true power when you combine its logic analysis capabilities with its built-in 200 Megasample/second 50 MHz bandwidth digitizing oscilloscope. You can quickly and easily measure total hardware performance — the effectiveness of digital hardware execution and the correct analog parametric

State listings provide necessary windows of address, data, status, and control line activity.



Time interval and event histograms let you view system hardware/software activity or specific modules for performance evaluation.



in one package...the new HP 1631A/D.

analog interactions with this logic analyzer.

results. In fact, you can now make many measurements that simply were impossible before. For example, now, in one instrument, you can examine digital system performance at the global level (system performance analysis), the functional level (state and timing analysis), and the parametric level (analog waveform analysis). All with the same powerful, yet easy-to-use instrument.

Easy peripheral expansion via HP-IB.

The new HP 1631A/D is a fully digitally-based, HP-IB compatible instrument. You can, for example, connect a single or dual disc drive for offline storage of test data and waveforms (the HP 9121D is shown, at $1270*). For easy permanent records of test data to include in reports, you can attach the new HP 2225A Thinkjet® printer ($495*).

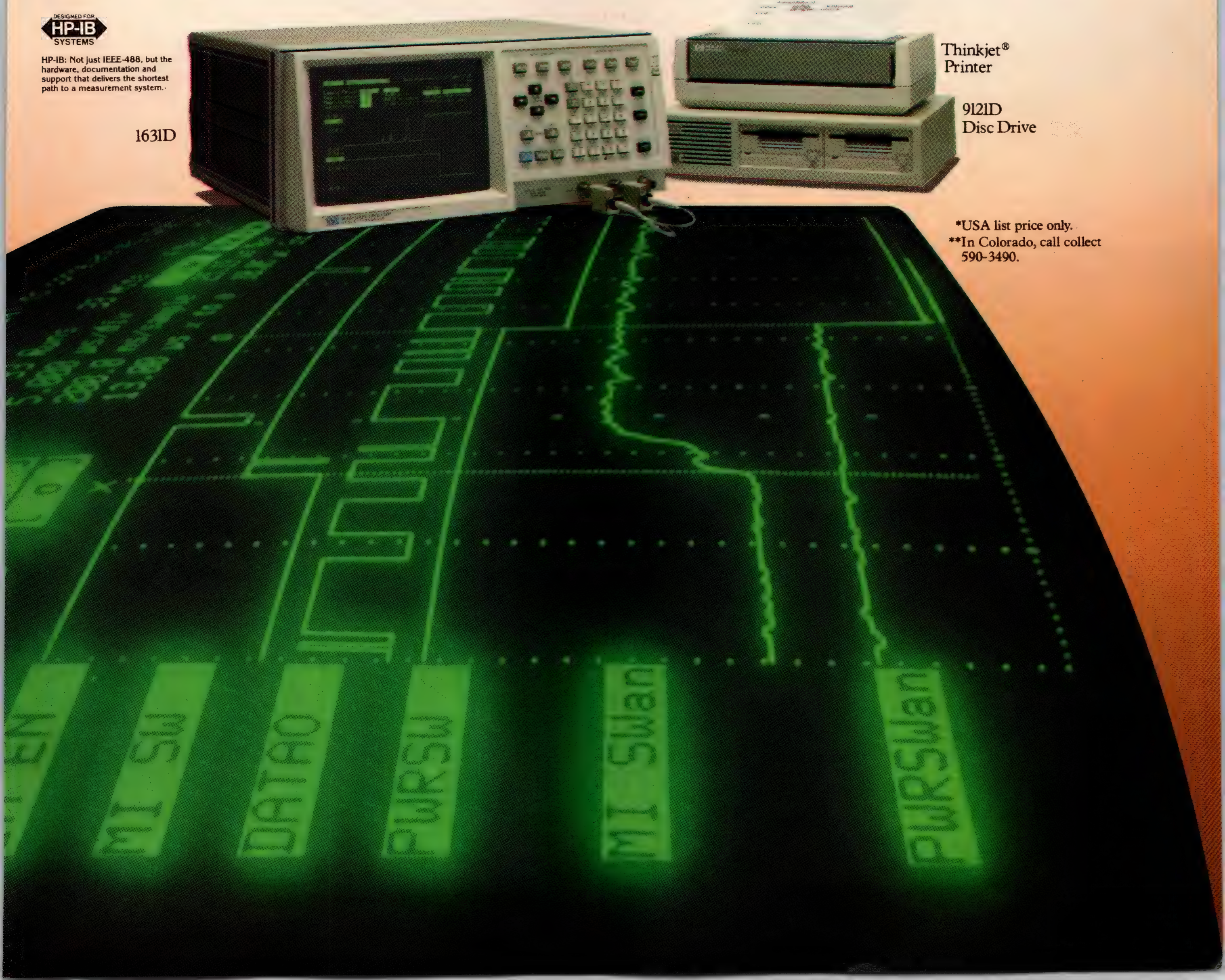
Call HP today. 1-800-835-5577.**

Call between 8:30 a.m. — 5:00 p.m. MDT for more information on the HP 1631A ($11,000*) or the HP 1631D ($13,000*). Or contact your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

HEWLETT PACKARD

CIRCLE NO 14

DS15509D



*USA list price only.
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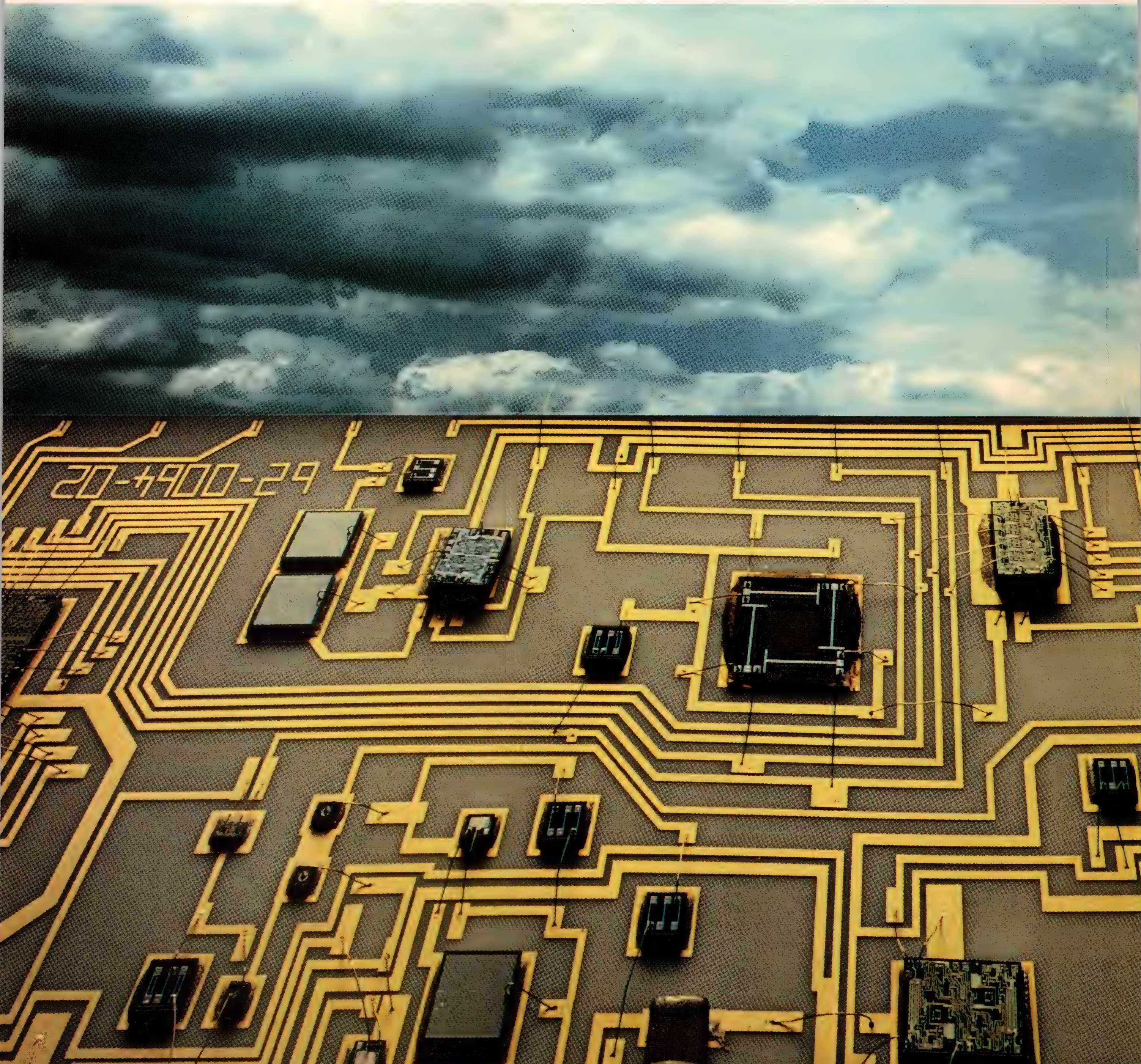
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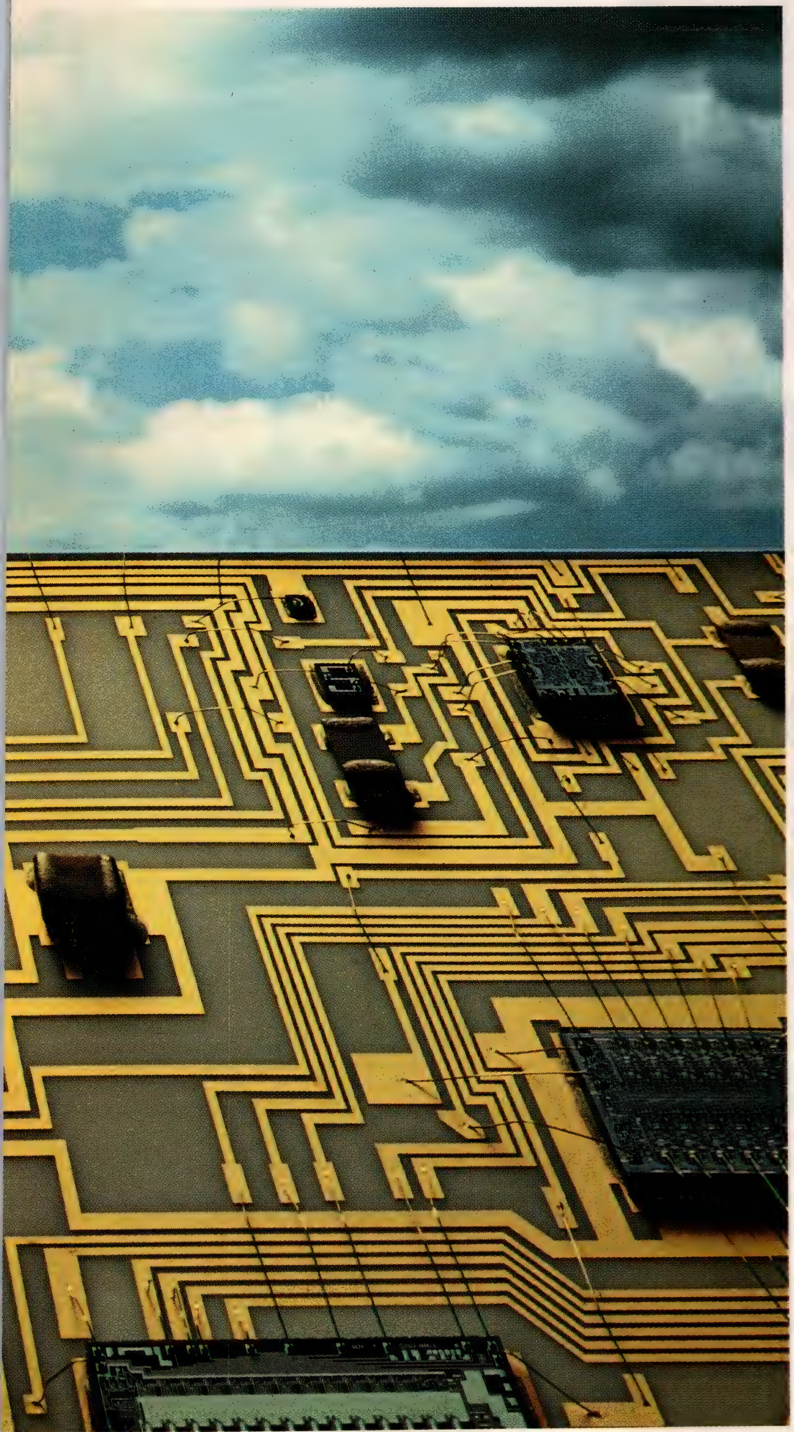
The Winds of Change



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Hybrid Systems: for over 20 years, we have worked closely with Design Engineers to generate change in the most demanding areas of high technology. Anticipating the needs of industry, we have created significant breakthroughs in precision data converters and data acquisition systems including the first 18–bit hybrid D/A converter, the first true 16–bit hybrid A/D converter, and the industry's smallest 12–bit, multi-channel data acquisition system. These innovations, and many more, have helped our customers transform their advanced ideas into impressive technological realities.

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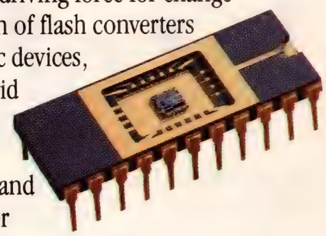

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CIRCLE NO 15

NEWS BREAKS

EDITED BY JOAN MORROW

FOUR CHIPS EXPAND THE TMS320 DSP FAMILY

Texas Instruments (Dallas, TX) has introduced four new digital-signal-processing chips: Three of them expand the capabilities of the TMS32010 branch of the TMS320 DSP IC family; the final chip begins another branch in that family. Executing op codes in a 160-nsec instruction cycle, the TMS32010NL-25 chip ($85) operates 20% faster than the original TMS32010 DSP chip. On the other hand, the TMS32011 chip ($85) provides a standard 200-nsec instruction cycle but it includes new, serial I/O capabilities. The TMS32010FNL chip ($75) supplies a standard TMS32010 in a plastic leaded chip carrier for surface-mount configurations.

Forming a new branch in the TMS320 family, TI's high-performance 32-bit TMS32020 DSP chip contains 544 words of on-chip RAM. By comparison, earlier TMS32010 DSP chips contain 144 words of RAM. You can equally divide the on-chip RAM so it contains both data and program-code blocks. Externally, the TMS32020 addresses a 64k-byte program memory and a 64k-byte data memory. More than 90% of the TMS32020's 109 instructions operate in a 200-nsec instruction cycle. The instruction set provides compatibility with the TMS32010's op codes and also furnishes 49 new instructions. Sample quantities of the TMS32020 in a 68-pin PGA package are available for $250 each.—Jon Titus

LOW-POWER CHIP SETS PROVIDE FAST NUMBER CRUNCHING

A CMOS-processed, 64-bit floating-point multiplier and a floating-point arithmetic logic unit (ALU) from Analog Devices Inc (Norwood, MA) offer 10^6 floating-point operations per second throughput and dissipate only 400 mW per chip. The ADSP-3210 multiplier and the ADSP-3220 ALU use a single pipelined design to deliver throughputs of 100 nsec for single-precision multiplication and single- and double-precision addition and 400 nsec for double-precision multiplication. The manufacturer claims the devices are the only floating-point units that can perform operations in three data formats: 32-bit, single-precision floating point; 64-bit, double-precision floating point; and 32-bit fixed point. Both chips comply with IEEE Standard 754 (Draft 10.0) for binary floating-point arithmetic.

To complement the arithmetic units, the company offers the ADSP-1401 program sequencer and the ADSP-1410 address generator. These ICs contain a look-ahead pipeline to minimize clock-to-address delays and to eliminate the need for external pipeline registers. The ADSP-1401 generates microcode memory addresses for implementing such sequencing operations as looping, jumping, branching, subroutines, condition testing, and interrupts. The ADSP-1410 has the ability to store and control interrupts on chip; the IC assigns priority to eight and two maskable external and internal interrupts (respectively), and asserts the interrupts in the cycle following their occurrence. The arithmetic chips come in pin-grid arrays; the sequencer and address generator are available in plastic or ceramic DIPs. The ADSP-3210 and -3220 cost $350 (100); the ADSP-1401 and -1410 are priced at $65 and $45, respectively.—Bill Travis

ECL ARRAYS OFFER HIGH INTEGRATION AND SPECIAL FEATURES

The Am3500 family of ECL gate arrays from Advanced Micro Devices (Sunnyvale, CA) comprises three products: the Am3500B standard 4988-gate array, the Am3550 5228-gate array with TTL- and ECL-I/O circuitry, and the Am3525 3500-gate array with 1152 bits of onboard RAM. The Am3500B and Am3550, which are the new devices in the family, contain the most logic of any ECL arrays; the Am3525 premiered in the

October 3, 1985, issue of EDN as the AmMPA3525. All arrays offer three speed-power options for their gates, the fastest of which specs 0.6-nsec worst-case switching time.

In addition to 5000 gates, the Am3500B and Am3550 include as many as 134 and 124 I/O cells, respectively. You can configure each of the I/O cells on the Am3550 to operate with pseudo-ECL (5V reference), true-ECL (−5.2 and 5V reference), or TTL signals. The true-ECL cells can also operate from −4.5 and 5V supplies.

To put your design on an Am3500 Series array, you create a net list and perform simulation using a commercially available workstation and the Texsim logic simulator. Advanced Micro Devices verifies your net list and performs physical design.—David Smith

DEGBUG HARDWARE, SOFTWARE SUPPORTS PROTECTED-MODE SOFTWARE

The AT Probe from Atron (Saratoga, CA, (408) 741-5900) lets you debug software written for 80286- and 80386-based PCs that directly address more than 640k bytes of memory. AT Probe provides standard hardware-assisted debugging features, including real-time trace; the protected-mode software package creates an environment that toggles between real-address and protected modes to handle development work. The software provides easy access to descriptor tables for the data structures to allow you to check and change data. The basic AT Probe costs $2495; the protected-mode software package costs $975.—Ed Teja

COLOR-PALETTE IC INCLUDES ON-CHIP D/A CONVERTERS

Allowing you to directly drive the red, green, and blue signals of a 75Ω video monitor via three 4-bit video D/A converters, the TMS34070 color-palette chip from Texas Instruments (Dallas, TX, (800) 232-3200) provides 16 colors per line in color bit-mapped display systems. You load the 4096-color palette directly from memory without processor intervention. Encased in a 22-pin, 400-mil plastic DIP, the chip offers a color look-up table that you can change on a line-by-line basis, video-speed D/A converters, two-to-one data multiplexing, automatic color-fill, and a vertical or horizontal color-retrace feature. Separate 5V power pins are provided for the analog and digital portions of the chip. The device operates at 36 MHz to control a matrix as large as 800×600 noninterlaced pixels; it costs $24 (100). You can also order a 20-MHz version, the TMS34070L-20, for $16.40 (100).—J D Mosley

SEMINAR WILL COVER DSP THEORY AND APPLICATIONS

A 4-day seminar entitled "Digital Signal Processing and Programmable Single-Chip DSP Processors—Theory, Design, and Applications" will be held on February 24 to 27 at the Royal Sonesta Hotel in Cambridge, MA. Along with discussions on such topics as digital signal processing and digital filter design, engineers and university professors will detail Texas Instruments' TMS32010 and 32020, Fujitsu's MB8764, NEC's μPD7720 and second-generation DSP processor, National's LM32900, Fairchild's PDF, and Kurzweil SC's KSC2408.

The $950 registration fee includes the book, Digital Filters and Signal Processing, as well as course notes, data sheets, and user manuals; a 10% discount is available to companies sending three or more people. The seminar will also be held on March 24 to 27 at Rickey's Hyatt House in Palo Alto, CA. For more information, contact Amnon Aliphas at DSP Associates, 18 Peregrine Rd, Newton Centre, MA 02159; phone (617) 964-3817.—Joan Morrow

One-micron CMOS breakthrough!

TRW LSI Products Division, the industry leader in high performance DSP products, has advanced the state-of-the-art in CMOS technology with the development of its OMICRON-C,™ one-micron CMOS process.

TRW's OMICRON-C represents a major breakthrough in CMOS manufacturing—producing one-micron CMOS in a bulk process. The challenge was to achieve the extremely advantageous CMOS combination of very high speed/low power, while improving latch-up immunity, a common problem to standard CMOS bulk process. TRW accomplished this by employing a retrograde p-well formation which permits shallower profiles and allows higher packing densities. Due to reductions in parasitic npn current gain, this technology controls the risk of latch-up far better than standard bulk process for the same geometry.

With TRW's OMICRON-C process, high volumes of quality chips can be produced at a competitive cost. This makes one-micron CMOS a feasible technology producing faster, cooler, more cost effective products in the future—but the future is now.

TRW LSI introduces the first commercially available chip utilizing one-micron CMOS technology—the TMC2110 multiplier-accumulator. It is a direct replacement for TRW's industry standard bipolar TDC1010 and can be used without circuit modification. The TMC2110 represents as much as a 2:1 increase in speed over previously available multiplier-accumulators, dissipates almost-zero static power associated with CMOS, but with total immunity to latch-up. Just look at these key features:

• 16-bit parallel multiplication with accumulation to 35 bits • 100ns multiply-accumulate time • Selectable accumulation, subtraction, rounding and preloading • Two's complement or unsigned magnitude operation • Single 5V power supply.

The TMC2110 is ideal for such high-speed, low-power applications as mini/microcomputer accelerators, array, video, radar signal and FFT processors. Available off the shelf through Arrow Electronics, Hall-Mark and Hamilton/Avnet.

Remember, you always get FULL SPEC PERFORMANCE from TRW LSI.

To learn more about our OMICRON-C breakthrough, one-micron CMOS process or to receive a TMC2110 data sheet, just call or write our Literature Service Department:

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NEWS BREAKS: INTERNATIONAL

BY PETER HAROLD

CARD LINKS MULTIBUS II SYSTEMS TO LOW-COST I/O BOARDS

Providing a link between Multibus II and the company's Z80-based Eurolog-bus, the MB2/LNK-1 board from Furrer-Gloor AG (Dietikon, Switzerland, TLX 58277) enables you to integrate low-cost, 8-bit industrial I/O into Multibus II systems. The link board provides 16k to 64k bytes of dual-ported RAM through which you can pass data and interrupt messages between the parallel system bus (iPSB) of Multibus II and the Eurolog-bus.

On the iPSB side, the board supports 8- and 16-bit data transfers, with the memory address of the dual-port RAM configured through interconnect space during system initialization. Interrupt messages received from the Multibus II system are converted into Z80 vectored interrupts on the Eurolog-bus, with the Multibus II interrupt source address readable from an interface register. The board, which costs approximately Sw fr 2000, will be available in June.

VME BUS BUBBLE MEMORY USES SCSI COMMANDS FOR ACCESS

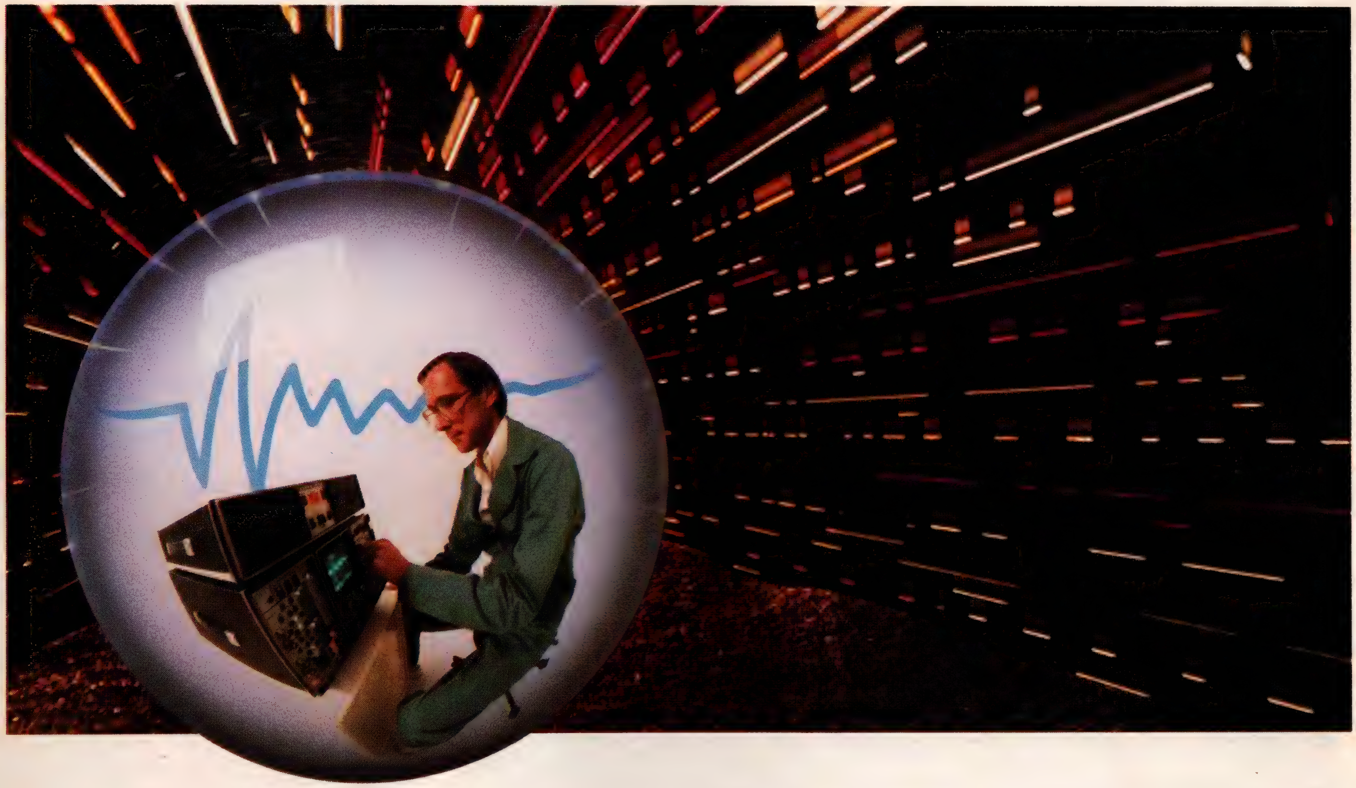
The PME-BB1 VME Bus bubble memory from Plessey Microsystems (Towcester, UK, TLX 31628) provides as much as 17M bytes of nonvolatile storage with an average access time of 11 msec (16 msec max) per 256-byte page. Furnishing a 1M-byte master card coupled to as many as eight 2M-byte slave cards via the P2 connectors, the system uses standard SCSI-type command blocks to access the data. Data is buffered into dual-port RAM on the master card and transferred over the VME Bus using an onboard DMA controller. You can perform 8- or 16-bit data transfers to acheive a VME Bus data rate as high as 2.6M bytes/sec for read operations or 3.6M bytes/sec for write operations. The master card costs approximately £3000; each slave card costs around £3500.

DISK CONTROLLER AND COMMUNICATIONS CARDS AVAILABLE TO OEMs

The intelligent disk and communication controller cards from Integrated Micro Products (Consett, UK, TLX 53429), which are used in the recently announced Unix-based Mentor microcomputer, are now available to OEMs. Designed for use on the VME Bus, the CT-68VIDC intelligent disk controller and the CT-68VICP intelligent communications card both have onboard 68000 μPs. The disk controller has an onboard DMA controller, a disk-cache buffer of as much as 512k bytes (or 2M bytes with an additional daughter board), and a SCSI Bus interface to support multiple Winchester disk, floppy-disk, or tape drives. The communications controller card also includes a dual-port RAM data buffer and provides 16 asynchronous serial I/O ports and 57 parallel I/O lines. Both boards sell for around $2000 each.

DSP CHIPS EXTEND DIGITAL-TV CAPABILITIES

Additions to the Digit-2000 digital-TV chip set from ITT-Intermetall (Freiburg, West Germany, TLX 772715) include a picture-in-picture processor, a double scan processor, and a video memory controller. The PIP-2250 picture-in-picture processor requires only two standard 16k×4 dynamic RAMs to allow you to overlay the main TV picture with a second one-third-size image and display it in one of four screen positions. The VMC-2260 video memory controller stores an entire picture frame in standard 64k×4 dynamic RAMs and provides freeze-frame, multiple picture-in-picture, and zoom capabilities, plus the ability to eliminate picture flicker by doubling the TV's vertical scan frequency. For the high-bandwidth color monitors required for teletext or computer display, where vertical scan frequency doubling is not suitable, the RGB-2932 double scan processor allows you to eliminate screen flicker by doubling the horizontal scan frequency of the RGB signals.



TIME MACHINES.

The Past. Nicolet digital oscilloscopes can record the history of your signal before the trigger point. Examine what preceded an event as well as the event itself. Use expansion to analyze the signal in detail at up to 100 times the resolution of an analog scope. Store the signals on floppy disk or bubble memory for future recall and reference. Or plot them out in report ready format.

The Present. Compare live signals with each other or with previously stored signals. Store any signal with the touch of a button and use voltage and time numeric display for exact comparisons. You can even display related signals as functions of each other instead of time. Manipulate waveforms using the scope's built-in programs or transmit them to a computer and back for display.

The Future. Expecting a transient? Set-up your Nicolet scope to capture it while you're away! Some models can even capture a sequence of events and store them on disk or bubble memory automatically ready for instant recall and display.

Get Results First Time, Everytime. Don't miss important data because of set-up error. Nicolet scopes are easy to use. Find out how they can be the quickest solution to your signal problems. For more information, write Nicolet Oscilloscope Division, 5225 Verona Road, Madison, WI 53711. Or call 608/273-5008.

Nicolet

For more information circle 2

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Model PLP

For complete specs,
refer to 1985-86 Gold Book
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Model PHP

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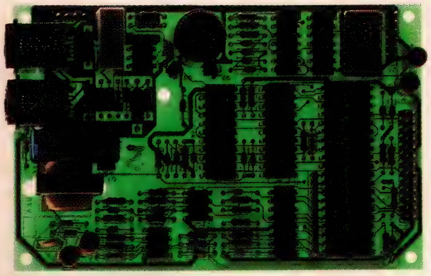
LOW PASS **Model PLP**	-50	-100	-150	-200	-300	-450	-550	-600	-750	-850	-1000
Pass Band, MHz (DC–)	48	98	140	190	270	400	520	580	700	780	900
20dB Stop Band start from	70	135	210	290	410	580	750	800	1000	1100	1340

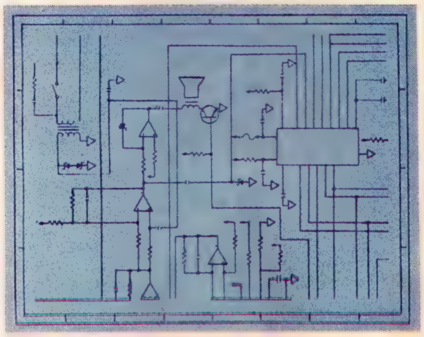
HIGH PASS **Model PHP**		-50	-100	-150	-200	-300	-400	-500	-600	-700	-800	-900	-1000
Passband, MHz	start	41	90	133	185	290	395	500	600	700	780	910	1000
	stop	200	400	600	800	1200	1600	1600	1600	1800	2000	2100	2200
20dB Stop Band, (MHz) from DC to		26	55	95	116	190	290	365	460	520	570	660	720

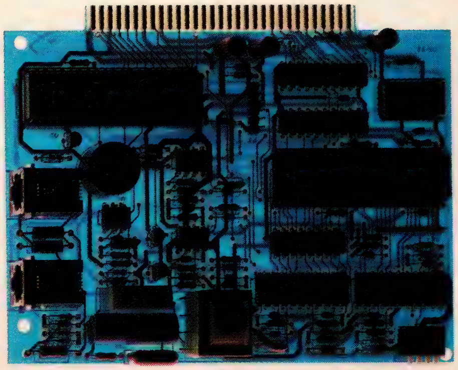
CIRCLE NO 16

F82-2 REV. ORIG.

absolutely, need reliable modems...







Customizing

your modem is your choice. From our standard off-the-shelf boards, to complete custom design, to licensing our proprietary CMOS chip design (for quantities in excess of 100,000 annually), we guarantee the right modem solution based on your deadline, design and volume requirements. Custom hardware configurations and firmware give you maximum freedom for integrating the modem into your overall product design.

Compact Size

is an important requirement in applications like credit check terminals, portable computers and trouble monitors. Ven-Tel modem density is state-of-the-art to provide excellent "real estate" value, with complete auto-dial/auto-answer, AT compatible, 212A modems—in as little as 12 square inches. With power requirements as low as 500mW.

Competitive Pricing

makes the Ven-Tel custom modem package one definitely worth looking into. For quotations based on your modem specs or a discussion with our experienced OEM sales engineers, call **800/538-5121 (outside California). In California, call 408/727-5721.** Or contact us for our custom modem brochure:
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2342 Walsh Avenue,
Santa Clara, CA 95051.

look at Ven-Tel

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Monolithic Memories

CIRCLE NO 18

SIGNALS & NOISE

Inventors should sign patents over to companies

Dear Editor:
I would like to comment on the article "Engineers who double as part-time inventors face full-time obstacles in the process" (EDN, October 3, 1985, pg 265).

Shortly before I graduated from Rutgers University, my brilliant electronics professor advised the class not to have second thoughts about signing away the rights to our inventions. He told us that he had patented several circuits on which he never made a nickel—which means, of course, that he lost money on the inventions. He told us a couple of stories illustrating the tremendous difficulties involved in administering a typical patent.

It's an economically sound idea for a big corporation to own a large number of patents, so it can be a strong force in markets for electronics, automobiles, aircraft, and other products. If every inventor with a couple of widgets creates his own little company—where, for instance, he designs a car around his widget—imagine all the energy these tiny companies will waste in feuding over administering their patents.

It's standard practice among large electronics companies to infringe on one another's patents. It saves a lot of litigation, and the sharing of the enormous pool of inventions improves the overall performance of the electronics industry. There are always a few malcontents around who want to satisfy their sense of importance by abolishing the present system entirely. But what about the sad side effects of the new system they propose?

Although I am content to feel that the patents I signed away are reflected in my professional status and salary, I would still endorse more equitable compensation for outstanding inventions—for instance, a percentage of the income they produce (which is very difficult to determine exactly in most cases). In addition, if a company doesn't use an invention for, say, five years, ownership of the patent should return to the inventor for the rest of the life of the patent.

Sincerely yours,
Otto H Bismarck
Fords, NJ

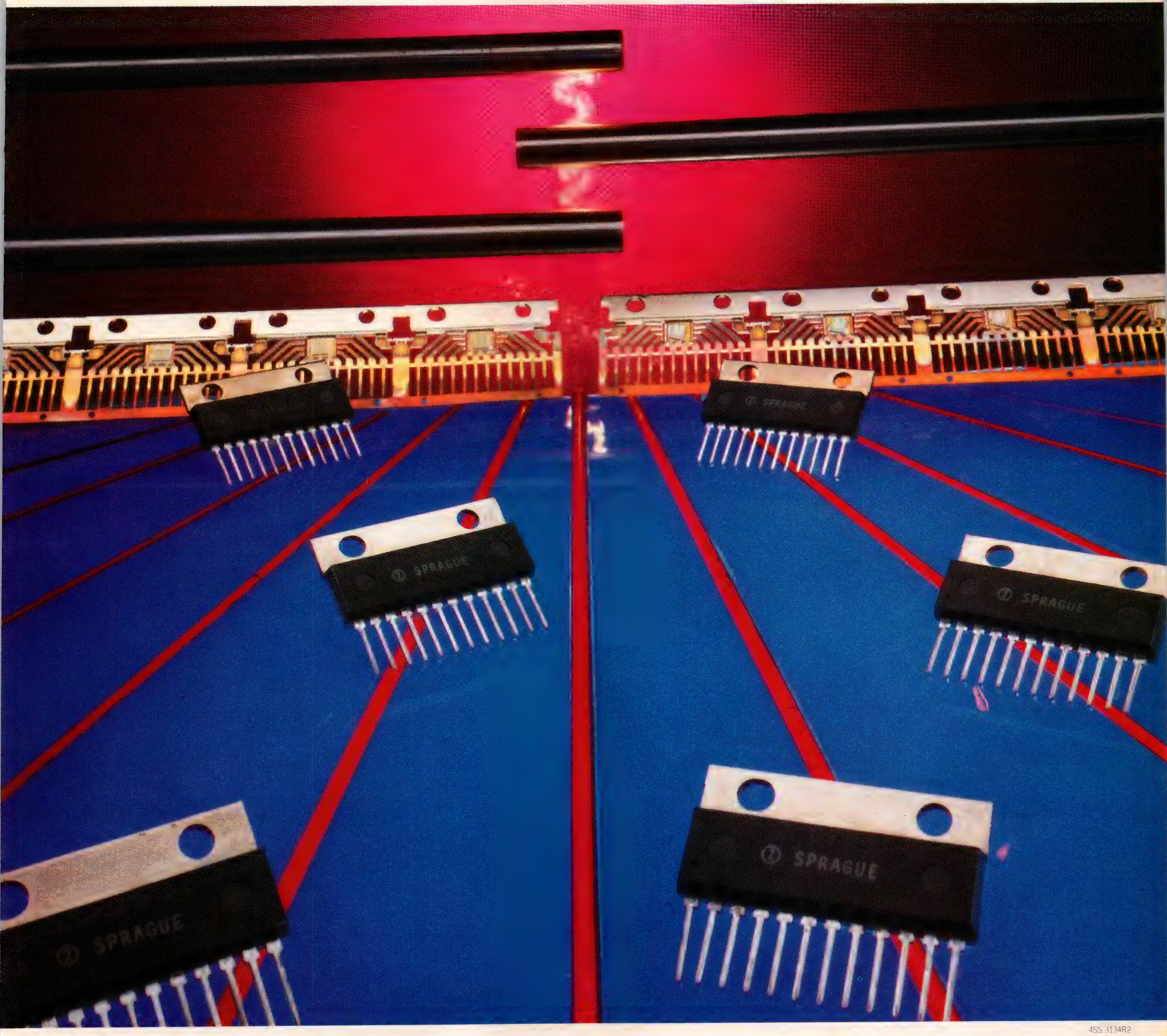
Willingness to take PE exam isn't enough

Dear Editor:
Vaso Bovan's letter in the October 31, 1985, issue of EDN (pg 25) mistakenly states: "All state registration boards give examinations once or twice a year for people who want to be PEs. There are no academic requirements . . . ."

This generalization is not true. In Missouri, there is a very specific requirement. In order to take the EIT or the PE exam, a person must have a *bachelor's* degree in engineering. Possessing a master's degree in engineering would not, of itself, qualify a candidate to take either exam. For such a candidate, the Missouri Board would make a determination as to whether the candidate's educational background were equivalent to a bachelor's degree in engineering from an accredited institution. Another exception exists for persons over 50 who have at least 20 years of engineering experience.

My own case provides a good example of the restrictions in such regulations. I have BS and MS degrees in physics and was a PhD-qualified candidate in physics before I took full-time employment. I have 20 years of technical experience in technical/educational fields, but am only 41. I am a member of IEEE and of Sigma Pi Sigma, the National Physics Honor Society. I've published papers in professional journals and have been employed as an engineer in industry for nearly

POWER HANDLERS.



4SS 3134R2

SPRAGUE DARLINGTONS SWITCH UP TO 1280W.

Sprague UDN-2878W and UDN-2879W Quad High-Current Darlington Switches provide a new level in power control capability. They serve as interface between low-level logic and high-power peripheral loads such as solenoids, motors, and incandescent displays. Capable of handling loads up to 320 W per channel, they are provided in 12-pin single in-line power tab packages. The inputs are compatible with most TTL, DTL, LS TTL, and 5 V CMOS logic. The UDN-2878W has an output voltage rating to 50V (35 V sustaining) while the UDN-2879W has an 80 V (50 V sustaining) rating. Volume pricing (50k) is just over $2. *Sprague Electric Company, a Penn Central unit,* Worldwide Hdqtrs., Lexington, MA. Write for Engineering Bulletin 29305.10 to Technical Literature Service, Sprague Electric Co., 41 Hampden Road, Mansfield, MA 02048-1807. For applications assistance, call Mark Heisig at 617/853-5000.

SPRAGUE
THE MARK OF RELIABILITY

CIRCLE NO 20

seven years, during which I've designed special-purpose computer systems, among other things. Yet, under Missouri regulations, I don't qualify to take either the EIT or the PE exam because I don't have an approved engineering degree.

I suspect that other states also have specific regulations that disqualify some would-be PEs. It's not simply a matter of being willing to take the exams.

Sincerely yours,
G M Hale
Metrology Engineering
Bendix Aerospace
Kansas City, MO

Overenthusiastic design

Dear Editor:

I really would like to say good things about the Design Idea "Tracking-load bank tests bipolar supplies" by David Bley (EDN, October 31, 1985, pg 252), because it's a good basic design that can draw ±1.5A from a ±19V supply or ±1.0A from a ±7 to ±25V supply. But it just can't draw ±1A from a 50V supply. If you try to make the LM317/337HVKs draw ±1A from a 50V supply, they won't be damaged or destroyed, but they'll go into current-limit and put out ¼ or ⅓A.

Unfortunately, I don't think there are any monolithic voltage regulators that can regulate 50V at 1A. (However, the LM12 will soon be able to handle 1.2A at 70V, or even more current, for a short time.) I'm afraid Mr Bley got a little overenthusiastic about the LM117's capabilities.

Sincerely yours,
Robert A Pease
Staff Scientist
National Semiconductor Corp
Santa Clara, CA

TEK SCOPE MAKES WORLD'S TOUGHEST SERVICE CALL.

On Mt. Everest you don't settle for second best. A scope has to be ready and able to measure under the toughest conditions on earth. For members of the Ultima Thule expedition, that meant a scope from Tektronix.

The team was on Mt. Everest to study the origins and effects of altitude sickness from research stations located at 17,000 and 21,300 feet. To accompany them they chose the Tek 2337 for its exceptional ruggedness and outstanding ease of use. Plus a well-earned reputation for no-compromise performance, no matter what.

Nothing stopped the scope from making its appointed measurements. Most impressive, it was used to troubleshoot, repair and calibrate medical test equipment that failed to operate at the 21,300-foot station.

Says spokesman Tom Clement, "Our research efforts were salvaged, at the highest and most critical altitude, thanks to the Tek scope."

For peak performance anywhere, depend on Tek's world-class family of portable scopes. Twelve scopes in all offering either analog or digital storage performance at bandwidths from 60 MHz to 300 MHz. Plus designed-in reliability that helps reduce your measurement costs.

To precisely match your needs, choose from three Tek 2000 family lines. The standard-setting, high-performance 2400 Series. The ultra-rugged 2300 Series. And the popularly-priced 2200 Series. All backed by Tek's 3-year warranty that includes the CRT.

To get your hands on a scope that goes where you go and doesn't scrimp on performance, contact your local Tek Sales Representative. Or call the Tek National Marketing Center toll-free:

1-800-426-2200.
In Oregon, call 1-627-9000.

Tektronix®
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CIRCLE NO 22

Anti-aliasing enhances measurement confidence. Signal distortion (sample mode only) is shown at high frequencies (top). The peak detect mode displays peak information without signal distortion (bottom).

INTRODUCING TWO DIGITAL STORAGE SCOPES WITH SOME MIGHTY IMPRESSIVE NUMBERS.

From 4K record length to 20 MS/s sampling at 100 MHz or 60 MHz... our two new scopes have just what you're looking for! The 2230 and 2220 are powerful digital storage oscilloscopes—and the first scopes in their class that include non-storage capability to these bandwidths.

You can reference, compare, and analyze waveforms with digital storage convenience, plus the confidence you get with analog measurements. Simply switch to the non-store mode to view the signal that the scope has digitized. Only Tek offers this flexibility to 100 MHz and 60 MHz in affordable scopes.

Enhancing use of the scopes as design and troubleshooting tools are fast sample and hold detector circuits, plus the proprietary peak detect mode. They enable the display of pulses as narrow as 100 ns at any sweep speed—even on a single sweep.

You'll also find such features as post-acquisition expansion and compression, X-Y capability to each scope's storage bandwidth and, for systems use, optional GPIB or RS-232-C interfaces.

Best of all, the 2220 and 2230 are easy to use and afford. And backed by Tek's famous 3-year warranty that includes the CRT. Check the front panels. The controls are familiar, comfortable, easy to identify. Designed to push productivity and minimize training time.

In the 2230, CRT readout of front panel settings and key parameters means even more convenience, with cursors for waveform voltage and timing measurements.

Get the reliability and performance you expect in Tek scopes, now enhanced by digital storage, at unexpected prices: $4150 for the 2220, $5150 for the 2230.

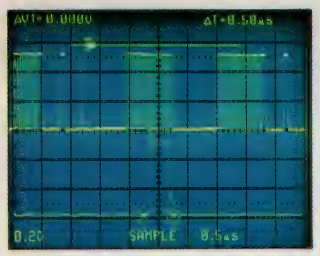
For the full story, and more impressive numbers, contact your local Tek Sales Representative today. Or call the Tek National Marketing Center,

1-800-426-2200.

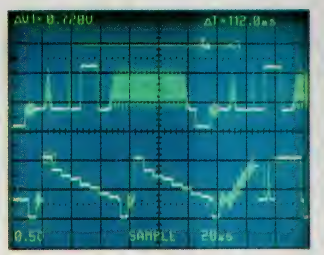
In Oregon, call collect,

(503) 627-9000.

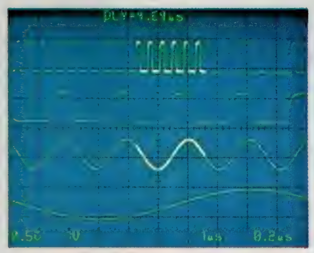
Features	2230	2220
Analog/Digital Storage Bandwidth	100 MHz	60 MHz
Single Shot (Transient) B.W. (10 points per signal period)	2 MHz	2 MHz
Maximum Sampling Speed	20 MS/s	20 MS/s
Record Length	4K/1K (selectable)	4K
Save Reference Memory	One, 4K Three, 1K	One, 4K
Vertical Resolution	8 bit 10 bit (avg mode)	8 bit
Peak Detect	Yes (100 ns)	Yes (100 ns)
Averaging	Yes (menu-selectable)	Yes (rep. sampling)
X-Y Storage Bandwidth	100 MHz	60 MHz
GPIB/RS-232-C Options	Yes (talker/listener, includes 26K of battery-backed memory)	Yes (talker/listener)
Price	$5150	$4150



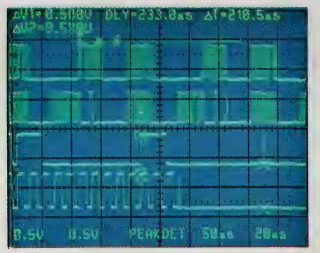
On-screen viewability lets you expand, compress, and position waveforms saved in reference memory. This permits easy viewing and display flexibility of up to eight saved waveforms.



High display resolution and accuracy permits on-screen viewing of signals such as the TV test signal shown here. 4K of record information can be viewed in 1K windows.



100 MHz, non-storage capability comes standard in the 2230. In addition, there's dual channel, dual timebase, versatile triggering and CRT readout.



The 2230 offers the convenience of CRT readout in both storage and non-storage modes at 100 MHz. Storage mode cursors make ΔV, ΔT, and 1/ΔT measurements fast and easy.

Tektronix
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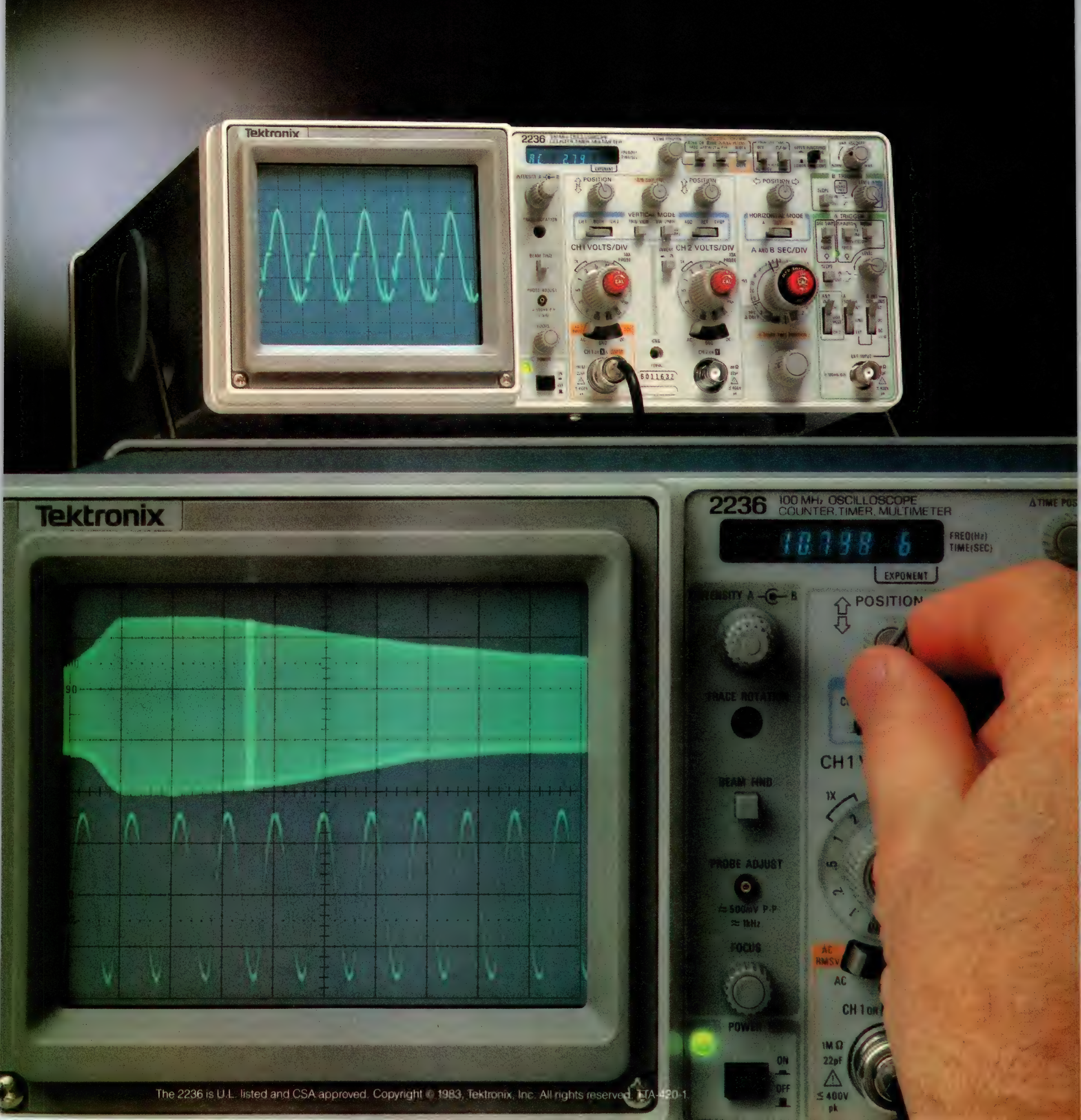
CIRCLE NO 61

DMM. Counter/timer. Easy, practical, more accurate measurements.



It's all within the scope of the Tek 2236!

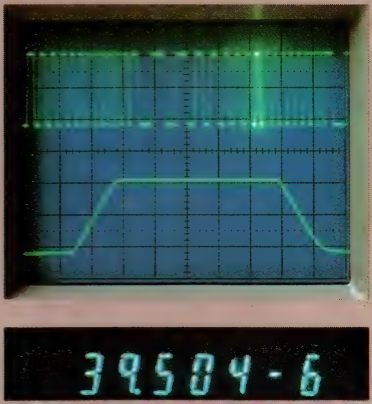
Precision measurements at the touch of a button. The 2236 combines 100 MHz, dual time-base scope capability with counter/timer/DMM functions integrated into its vertical, horizontal and trigger systems.

For the same effort previously required just to display the waveform you can obtain digital readout of frequency, period, width, totalized events, delay time and Δ-time to accuracies of 0.001%.

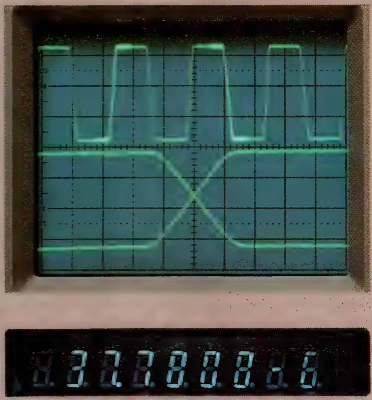
Practicality is the cornerstone of the 2236. The 2236's intensified on-screen markers make gated counter measurements easy, with no mental arithmetic required. And the 2236 offers an independent floating 5000 count auto-ranging multimeter with side inputs for DC voltage measurements to 0.1%. An auto-ranging ohmeter provides resistance measurements ranging from 0.01Ω to GΩ—as well as audible continuity. Operator prompts, auto-ranging and audible, automatic diode/junction detection features serve to simplify set-up and enhance confidence in your measurements.

Left top: Ch 1 true RMS & DC volts measurements. Made easily at the probe tip. (The 2236 adjusts automatically to 1X or 10X probes.) The 2236 includes relative reference capability for subtracting offsets.

Left bottom: Gated frequency measurement. Intensified zone brackets the period of interest by means of the delayed sweep, allowing easy frequency measurement on any specified portion of the waveform.



Gated width measurement. Pulse of interest is selected with the intensified zone. Both width and period measurements are made with up to 10 ps resolution.



Delta time measurement. Time between two intensified zones on the A sweep is measured with up to 50 ps accuracy.

You can obtain scope, counter and DMM input simultaneously through a single probe. The same probe is used to provide input for the 2236 CRT display and the digital measurement system resulting in easy set-up, greater measurement confidence and reduced circuit loading. You can make direct digital measurement of dc volts and ac coupled true RMS volts through the Ch 1 input.

And the 2236 is backed by the industry's first three-year warranty on all parts and service—including the CRT. To learn more, contact Tektronix:

U.S.A., Asia, Australia, Central & South America, Japan
Tektronix, Inc.
P.O. Box 1700
Beaverton, Or 97075
TWX: 910-467-8708
TLX: 15-1754
Cable: TEKTRONIX

Europe, Africa, Middle East
Tektronix Europe B.V.
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1180 AV Amstelveen
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Telex: 18312-18328

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CIRCLE NO 100

CALENDAR

PL/M-86 Systems Programming (short course), Madison, WI. Donna Miller, Micro-Managers Inc, 1435 E Main St, Madison, WI 53703. (608) 251-6661. February 3 to 7.

EMI Control in Computers and Printed Circuit Boards (short course), San Jose, CA. Penny Caran, Interference Control Technologies, State Rte 625, Box D, Gainesville, VA 22065. (703) 347-0030. February 4 to 7.

Grounding and Shielding (short course), Orlando, FL. Penny Caran, Interference Control Technologies, State Rte 625, Box D, Gainesville, VA 22065. (703) 347-0030. February 4 to 7.

UniForum, Anaheim, CA. /Usr/Group, 4655 Old Ironsides Dr, Suite 200, Santa Clara, CA 95054. (408) 986-8840. February 4 to 7.

iRMX 86 for Users (short course), Madison, WI. Donna Miller, Micro-Managers Inc, 1435 E Main St, Madison, WI 53703. (608) 251-6661. February 10 to 14.

Grounding and Shielding (short course), San Antonio, TX. Penny Caran, Interference Control Technologies, State Rte 625, Box D, Gainesville, VA 22065. (703) 347-0030. February 18 to 21.

IEEE Annual Meeting, San Jose, CA. IEEE, 10th Fl, 345 E 47th St, New York, NY 10017. (212) 705-7647. February 18 to 19.

AutoCADCon 86, Rosemont, IL. CAD Design Systems Inc, 1305 Remington Rd, Suite D, Schaumburg, IL 60195. (312) 882-0114. February 20 to 21.

C Programming Workshop, Bellevue, WA. Specialized Systems Consultants Inc, Box 55549, Seattle, WA 98155. (206) 367-8649. February 24 to 28.

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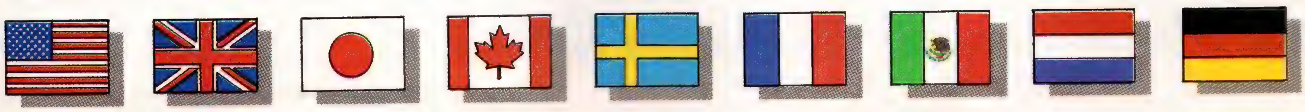

CIRCLE NO 25

CALENDAR

Nepcon West '86, Anaheim, CA. Banner and Greif, 110 E 42nd St, New York, NY 10017. (212) 687-7730. February 25 to 27.

Compcon Spring, San Francisco, CA. IEEE Computer Society, 1730 Massachusetts Ave NW, Washington, DC 20036. (203) 371-0101. March 3 to 6.

First International Conference on CD ROM, Seattle, WA. Microsoft Corp, Box 97200, Bellevue, WA 98009. (206) 828-8080. March 3 to 6.

Dexpo Europe 86 (DEC-Compatible Exhibition and Conference), London, UK. Expoconsul International Inc, 3 Independence Way, Princeton, NJ 08540. (609) 987-9400. March 4 to 6.

Power UK '86, London, UK. TCM Expositions Ltd, Exchange House, 33 Station Rd, Liphook, Hampshire, GU30 7DN, UK. (0428) 724660. March 4 to 6.

Design/Drafting with Surface Mount Devices (short course), Milwaukee, WI. Peter Tocups, University of Wisconsin-Milwaukee, 929 N 6th St, Milwaukee, WI 53203. (414) 224-3952. March 5 to 7.

7th Annual Computer Graphics Conference, Hollywood, FL. Frost & Sullivan, 106 Fulton St, New York, NY 10038. (212) 233-1080. March 5 to 7.

CAD/CAM/CAE Winter Workshops, San Diego, CA. Jack Sanders, CAD Report, 841 Turquoise St, Suite D, San Francisco, CA 92109. (619) 488-0533. March 6 to 7.

CIMTECH '86, Boston, MA. Society of Manufacturing Engineers, Box 930, Dearborn, MI 48121. (313) 271-1500. March 10 to 13.

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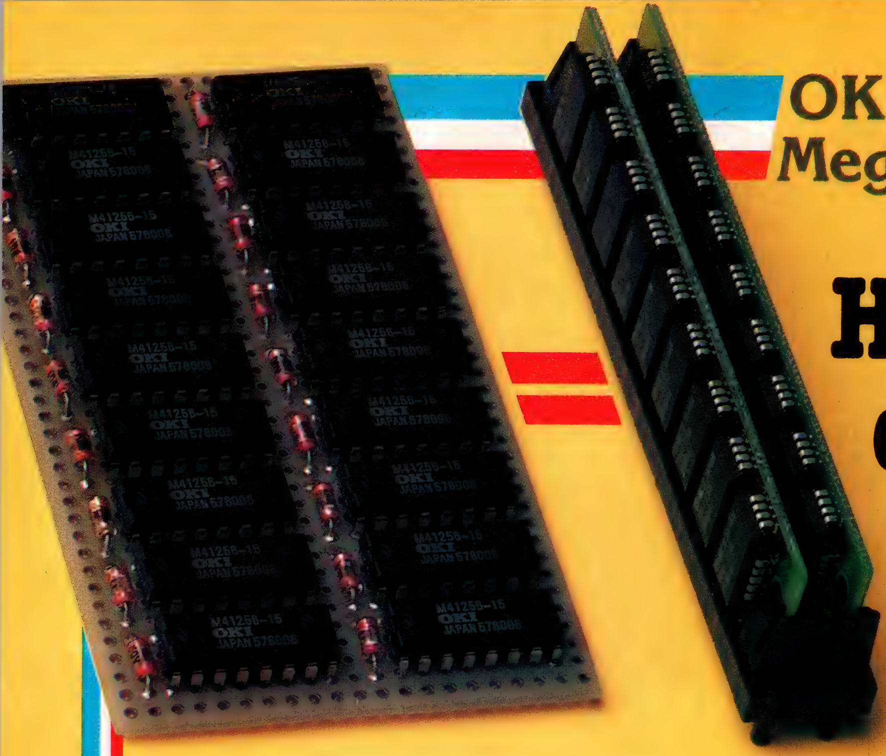
CIRCLE NO 27


2 MICRON CMOS.
HI-REL ASIC.
Siliconix
incorporated
Siliconix incorporated, 2201 Laurelwood Road, Santa Clara, CA 95054, (408) 970-4107 TWX 910-338-0227



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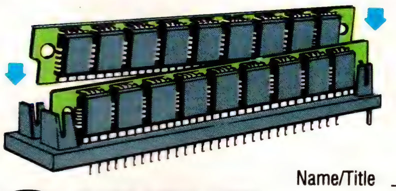

☐ Please send____ OKI DRAM SIMM Sample Set(s) with socket. Price per set is $44.00, plus $4.00 for shipping/handling: $48.00 Set/total, sales tax included. Offer limited to 3 sets per customer.

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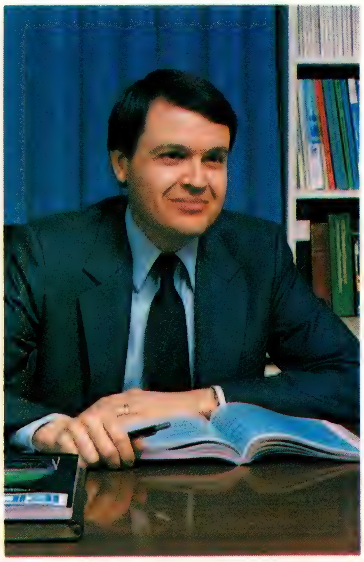
EDN

Smart vendors address market needs



The only successful products are those that provide benefits. Personal computers, for example, can make correspondence or circuit design easier. Application-specific ICs (ASICs) can reduce space requirements, power consumption, and costs. A benefit to one person, however, may be nothing at all to someone else. It's all too easy for us, as engineers, to produce products that *we* think are desirable without considering the requirements of the marketplace.

Creators of local-area networks might well be guilty of just such a misjudgment. For the last several years, while they've been trying with only limited success to sell LANs in labs and offices, an important market for LANs has developed in factories. The LAN vendors haven't ignored the factory market, of course, but they seem unable to grasp an important requirement for selling to that market: the requirement for all types of hardware to communicate. The smaller scale of an office or lab allows the use of one, or at most a few, types of hardware; it's not much of a disadvantage if that hardware can't communicate with other hardware. A factory, however, is different: The numerous manufacturing operations require equipment of all sorts. Whereas LAN standards are merely desirable for the office, they're absolutely necessary for the factory.

General Motors, recognizing the benefits of standards, has taken a strong lead. "Adhere to the MAP [Manufacturing Automation Protocol]," it tells equipment suppliers, "or we won't buy from you." Other large manufacturers, who stand to benefit from GM's initiative, are supportive. The result, if all goes as expected, will be a standard that's driven not by equipment suppliers—as is the case with vendors' faltering efforts to put networks in offices—but by users.

The potential benefits of standard factory LANs are enormous. At a time when American manufacturers are struggling to maintain position in the world market, standard LANs can increase efficiency and enhance competitiveness, perhaps even make a major impact on the American economy. Clearly, the marketplace is crying for standard factory LANs. Belatedly, electronics suppliers are fulfilling the needs of the marketplace rather than catering to their own desires.

Gary Legg

Gary Legg
Editor

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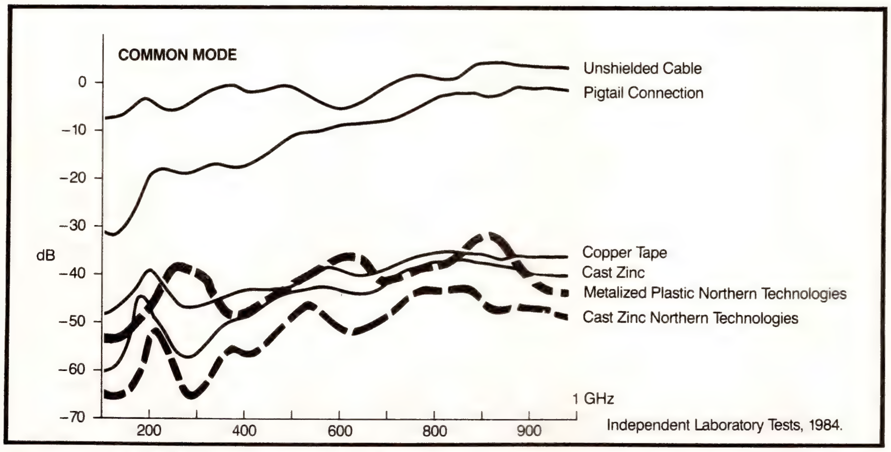

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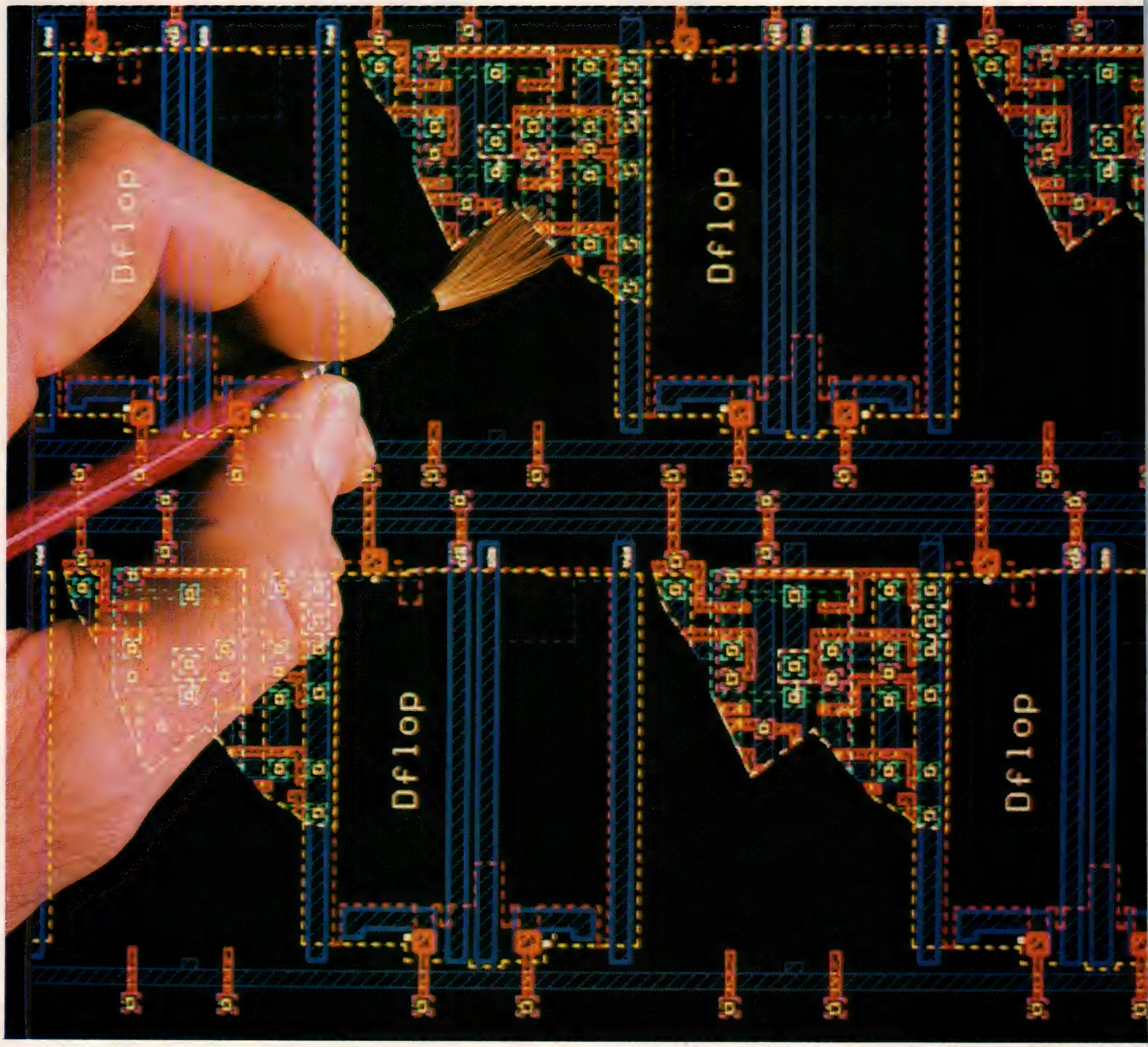

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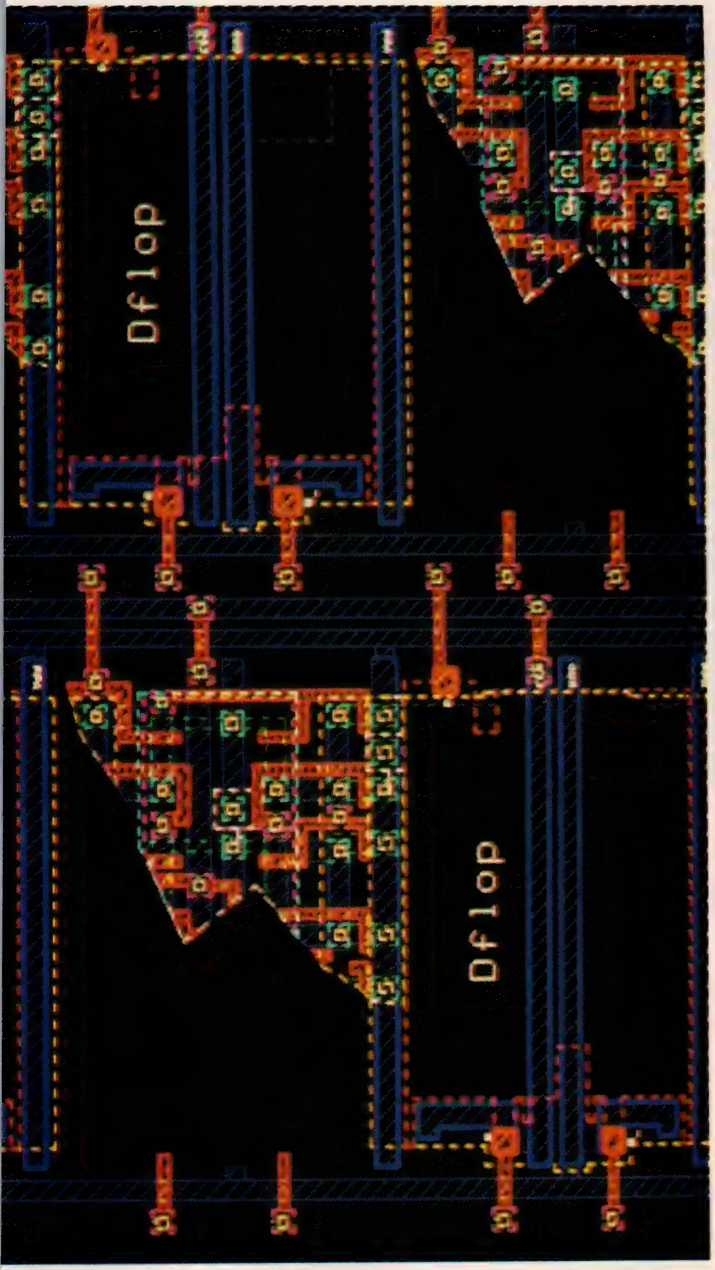

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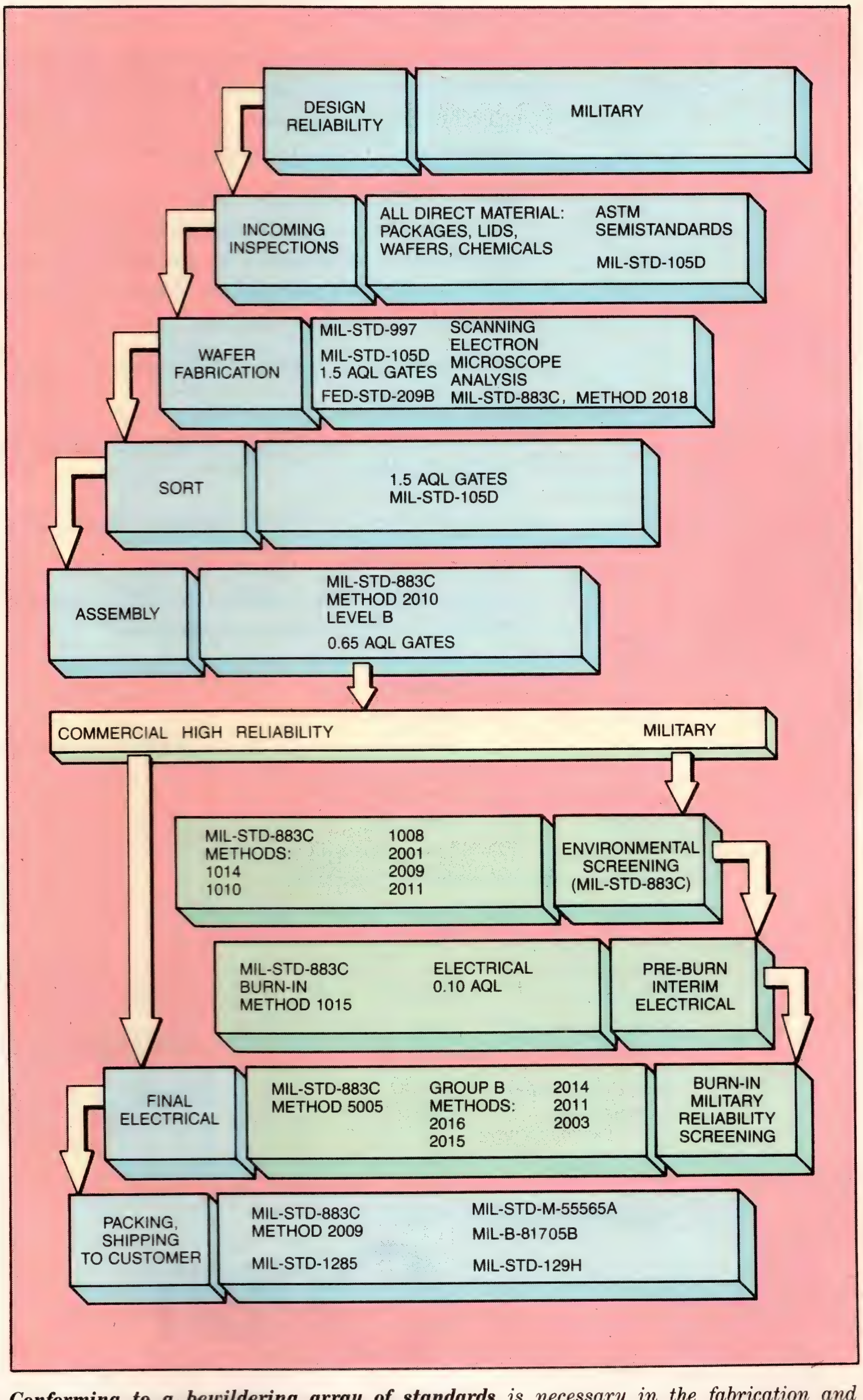
CIRCLE NO 31

Semicustom ICs for military use meet rigid reliability specs

David Smith, *Associate Editor*

Recognizing the lucrative and stable military market, semicustom-IC vendors offer digital arrays, linear arrays, and standard-cell ICs that can meet MIL-STD-883C reliability standards. The devices can be used in designs that require as many as 24,000 logic gates or that must operate at clock rates in the hundreds of megahertz. In addition, vendors are beginning to characterize their products for radiation hardness, and they are discovering that bulk silicon can provide radiation immunity. In fact, most applications don't require the more expensive rad-hard technologies like GaAs and silicon on sapphire.

The design and fabrication of military semicustom ICs is similar to the development of commercial products (see **box**, "Developing military semicustom ICs"). To offer their products for the military markets, vendors need to implement the testing, screening, and documentation procedures required by military specifications (for a description of the military standards for ICs, see **Ref 1**). These procedures add to the cost of producing military semicustom ICs (see **box**, "The cost of military semicustom ICs"). To consider using semicustom ICs in your project, determine if you can afford the development costs, then take a look at the performance and integration levels of available product lines.



Conforming to a bewildering array of standards *is necessary in the fabrication and screening of military semicustom ICs. This manufacturing flowchart from AMCC shows the company's manufacturing steps and the military specifications required at each. The three steps under the label "MILITARY" (upper right) are not performed for commercial arrays. These additional steps and more expensive packages can increase the price of military semicustom ICs 100 to 200% over commercial products.*

ICs must withstand radiation

In addition to undergoing MIL-STD-883C screening, many military ICs must meet stringent radiation-hardness criteria. Some manufacturers suggest that within a few years all military ICs, including semicustom chips, will require a

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Double poly start to completion	15	8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
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25 cut and goes	1	18 23

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CIRCLE NO 33

Developing military semicustom ICs

The design of military ICs is generally similar to that of commercial devices. The dissimilarities occur in the fabrication and testing of the ICs, in which the military dictates stringent testing requirements. The IC manufacturer must have the facilities and procedures in place and qualified before he can guarantee that your ICs meet military standards.

During design, you must take into account the wider temperature range of military applications. In the accompanying article, the effect of temperature on predicted performance is shown in several of the examples. In addition, high levels of radiation can degrade the performance of ICs by as much as 50%. You need an estimate of the performance degradation under the level of radiation required by your project. The degradation caused by radiation must be included with degradation from voltage and temperature variations in your timing simulations.

Testing requirements of military ICs are more stringent than those for commercial ICs because military specs often dictate a specific level of fault coverage. For example, a draft of Air Force regulations regarding microcircuits requires that test vectors detect 95% of all possible faults on an IC. Commercial devices, on the other hand, might require only functional and ac verification. You should have fault simulation included in your design process to allow you to verify the level of fault coverage provided by your test vectors.

Prototype semicustom ICs might not require full screening to verify the operation of a prototype system, but the chips intended for use will take considerably longer to qualify than commercial ICs. The extensive screening requirements add weeks to the delivery schedule of military ICs. For example, if your application requires that the manufacturer burn-in your ICs for 1000 hours, then you add almost seven weeks to the delivery of the chips. Manufacturers of standard parts can screen ICs before you need them and deliver them upon receipt of order.

When choosing a military-IC supplier, you have to consider more than gate density and product-line performance. Dale Wilson, sales manager of Circuit Technology Inc's IC Div, lists other factors: military circuit experience, design and manufacturing documentation, in-house screening and qualification facilities, provision for customer and government inspections, and assembly controls and quality-assurance functions. These factors are necessary to ensure that you can monitor the entire chip-development process, from design documentation through final electrical test, to both the government's and your satisfaction.

demonstrated immunity to radiation. Currently, the most stringent criteria sets the total dose of radiation at 10^6 rads. This criteria would hold for ICs subject to nuclear blasts. Similarly, most space applications, such as the Galileo probe to Jupiter, must meet a radiation tolerance of at least 10^5 rads. Other military systems not subject to direct nuclear-bomb blasts or radiation in space may not need to meet these levels of radiation hardness.

For the radiation-intensive applications, substrate materials other than bulk silicon can offer higher tolerance to radiation. Both silicon-on-sapphire (SOS) and GaAs technologies exhibit radiation immunity as high as 10^8 rads. RCA Solid State, Circuit Technology Inc, and Asea Hafo offer semicustom ICs that use CMOS SOS processes. Manufacturers of GaAs semicustom ICs appear in **Ref 2**. These technologies are best for applications requiring very high immunity to radiation, and they are more expensive than bulk-silicon products.

Suppliers test for rad hardness

Many suppliers of semicustom ICs are now undergoing or have completed tests to determine the radiation hardness of their products. For example, Honeywell specifies that its HM Series bipolar arrays and its HC Series CMOS arrays withstand 10^6 rads. Applied Micro Circuits Corp (AMCC) offers ECL arrays that tolerate a total dose of 7×10^6 rads and conform to MIL-STD-883C. To simplify the design of its arrays, AMCC offers its Macromatrix CAE software for Daisy, Mentor, Valid, and Tektronix workstations. The software includes logic macros, a net-list translator to convert the workstation format into AMCC's format, a test-pattern formatter, engineering-rules checkers, and an annotation program for including layout delays in logic simulations.

Another manufacturer of radiation-hardened arrays is Fairchild, whose FGC and FGE Series devices have recently been specified at the 10^6-rad level. Measured under the supervision of US Army personnel, six devices from each series operated within functional specifications after total doses of 10^6 rads; in addition, two devices from each series sustained exposure to 2×10^6 rads without failure. Another measure of radiation hardness, dosage-rate (transient) hardness, specifies an IC's ability to withstand transient

radiation bursts lasting between a few and hundreds of nanoseconds. The FGC arrays withstand 5×10^8 rads/sec of transient radiation; the FGE arrays withstand 5×10^{10} rads/sec.

For military applications requiring low power consumption, therefore, the CMOS FGC arrays can meet most radiation-hardness specs. Arrays in the series contain between 540 and 6000 equivalent 2-input gates, and Fairchild estimates that you can use 80% of the available gates in a typical design. The arrays support clock rates as high as 50 MHz typ, and because devices spec'd over the military-

The cost of military semicustom ICs

Military semicustom parts have price policies similar to those of commercial gate arrays. You pay a nonrecurring engineering (NRE) charge for development, fabrication, and assembly of your chips. The NRE charge includes a few prototype chips (usually between 25 and 50) for test and verification. The manufacturer performs dc tests and often critical-path ac tests but does not perform extensive characterization and screening as part of the NRE price. Prototypes don't always need the full screening required by production chips for finished products, so the vendors keep these charges optional in case your prototype systems need to meet only functional specifications.

To clarify the pricing policy of its military products, Siliconix announced a 5-point program in December for its 3- and 5-µm CMOS gate arrays. The program guarantees certain price and delivery schedules and thereby eliminates some typical ambiguities inherent in customer-designed products. First, Siliconix provides its design tools free to customers who agree to develop an IC with the company. Next, the NRE charge is firm, barring changes that affect more than 10% of the work already completed. Third, the company guarantees a delivery date provided you guarantee to bring the design into production. Fourth, the NRE charge provides for 100 prototype ICs, often enough for an entire military program. Finally, the company guarantees a mask-level second source.

Hughes Aircraft supplies potential customers with an estimate of gate-array development costs. The figures are not specific charges but rather guidelines to help you estimate costs before you devote time to writing a formal request for quotation (RFQ). Hughes states that only a formal RFQ results in a firm price estimate, and the RFQ must include chip characterization and screening requirements in addition to design considerations.

The basic NRE charge for a Hughes array ranges from $30,000 to $100,000. The wide variation is caused by the variety of technologies and array sizes offered by the company. The charge includes workstation software for design and simulation, design verification, placement and routing, production of masks for IC fabrication, wafer fabrication, and prototype assembly. In addition, the NRE charge covers the development of a test program that can range to as many as 4000 test vectors and six critical-path ac tests. Computer time for simulation and for placement and routing is also included, as is eight hours of consultation with the company's engineers. If you need to make a second pass of your design after prototype fabrication, you can expect to pay between 60 and 100% of the original NRE charges.

Hughes lists several additional charges for array development that you might incur, depending on the requirements of your design. For example, if you have Hughes burn-in your ICs, you'll pay between $800 and $1500 for burn-in boards that contain between six and 30 sockets for ICs. Consultation beyond the eight hours in the NRE charge costs $800 a day, and test vectors beyond 4000 cost $10 each. If Hughes develops a special macrocell for your design, the company charges between $5000 and $20,000, depending on cell complexity. Hughes can produce detailed documentation of the development and manufacture of your IC for $5000 to $15,000. Finally, military qualification according to MIL-STD-883C subgroups A, B, C, and D costs $9500 plus the cost of destroyed samples, typically $300 to $400 each.

Because military parts require more screening than commercial parts, they cost more. Also, military temperature and stress requirements almost always necessitate the use of expensive packages. As a result of variations in screening and packaging costs, military semicustom-IC suppliers often decline to estimate the typical cost of production ICs until they get an RFQ and manufacturing-volume estimate. Those who do comment on unit costs estimate that military semicustom ICs cost two to three times as much as commercial ICs once in production. Hughes's guidelines quote production-IC unit cost between $150 and $700, depending on quantity, utilization of available gates, and processing technology, in addition to packaging and screening flow.

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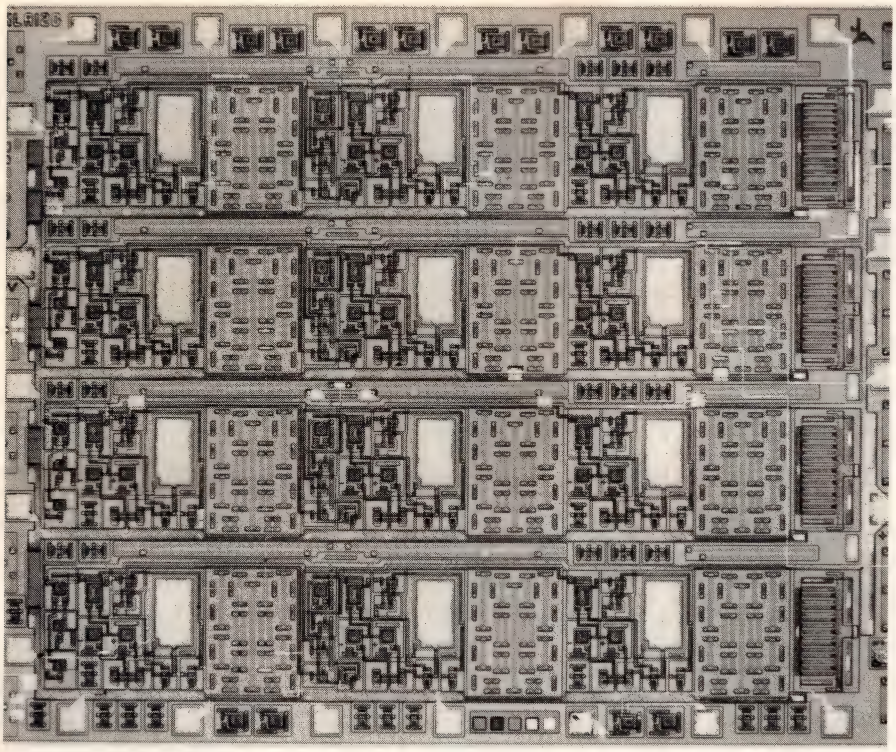

Macrocell gain blocks implement op amps or comparators on Raytheon's RLA120 linear array. You specify the layout for each block (dotted line) to determine if it operates as an op amp or as a comparator.

temperature range exhibit gate delays 83% longer than those of commercial devices, the arrays should support a 27-MHz (50 MHz÷1.83) clock frequency over the military-temperature range. Fairchild estimates worst-case power consumption of the arrays to be 1W.

For applications requiring high speed, the ECL FGE Series arrays can support clock frequencies as high as 600 MHz typ. The four products in this series contain between 100 and 2840 equivalent 2-input gates and between 21 and 120 I/O circuits. They can operate in both 10K and 100K ECL circuits, and the largest array, the FGE2500, can also interact with TTL-level circuits. The cell library for the FGE Series contains cells with varying speed and power specifications, allowing you to save power in the parts of your design that don't require the maximum speed of the array. Still, the largest arrays dissipate between 4 and 8.5W, necessitating the use of a heat sink on the chips' pin-grid-array packages.

Fairchild offers two advantages for military designers who need fast turnaround of semicustom-IC prototypes. First, the company uses an in-house Cray 1-S2000 supercomputer for logic and fault simulation and for layout design. The supercomputer speeds the simulation and layout of gate arrays; for example, a 2000-gate ECL array fault simulation that requires 48 hours on a VAX 11/780 computer requires only one hour on the Cray. Similarly, automatic placement and routing of a 6000-gate CMOS array takes 15 minutes on the Cray, vs three hours on the VAX.

E-beam speeds prototyping

The other advantage Fairchild offers is its electron-beam (E-beam) lithography system. The E-beam system writes the pattern of a particular layer onto a wafer's photoresist material, eliminating the need for the masks required with optical-lithography systems. By skipping the mask-making step, the E-beam system reduces prototype turnaround time by two weeks or more. Depending on backlog, Fairchild hopes to turn around ECL array prototypes in two weeks. Similar turnaround times for CMOS designs should be available this year. For comparison, manufacturers typically claim to deliver prototypes in six to 10 weeks.

Offering the highest level of integration for military applications, U Series CMOS gate arrays from Hughes Aircraft contain between 1040 and 40,000 equivalent 2-input gates. These arrays use a channelless (sea-of-gates) architecture that contains no dedicated wiring channels. The company's layout software dynamically assigns wiring channels as it connects macros using an interconnect grid within each array's cells. Therefore, some of the cells contain only wiring, and others implement macros. The company claims to use 60% of the available gates for logic, so for the largest array in the series you can implement the equivalent of 24,000 2-input gates.

U Series arrays spec internal gate delays as short as 400 psec, and counters on the arrays can operate at frequencies as high as 200 MHz. They offer as many as 248 I/O pins, and the output buffers can drive six TTL loads. Turnaround time for these arrays averages eight weeks.

Hughes also offers a line of CMOS gate arrays that use a more conventional architecture. This line, the Quad Logic Array family, contains four arrays that provide 2000 to 8000 equivalent 2-input gates. The Quad Logic name describes the basic cell in the array, which contains two 2-input and two 3-input gates, resulting in an architecture that, according to the company, minimizes the number of gates per macro function and maximizes routing efficiency. Delay of internal gates is 1.4 nsec, supporting clock rates as high as 35 MHz typ. At 125°C, performance degrades 30%; a 10% drop in supply voltage (from 5.0 to 4.5V) slows the array circuit-

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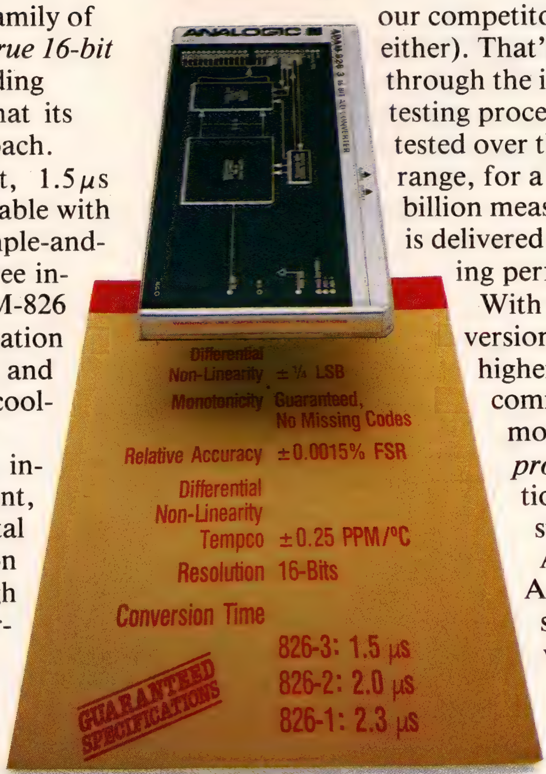

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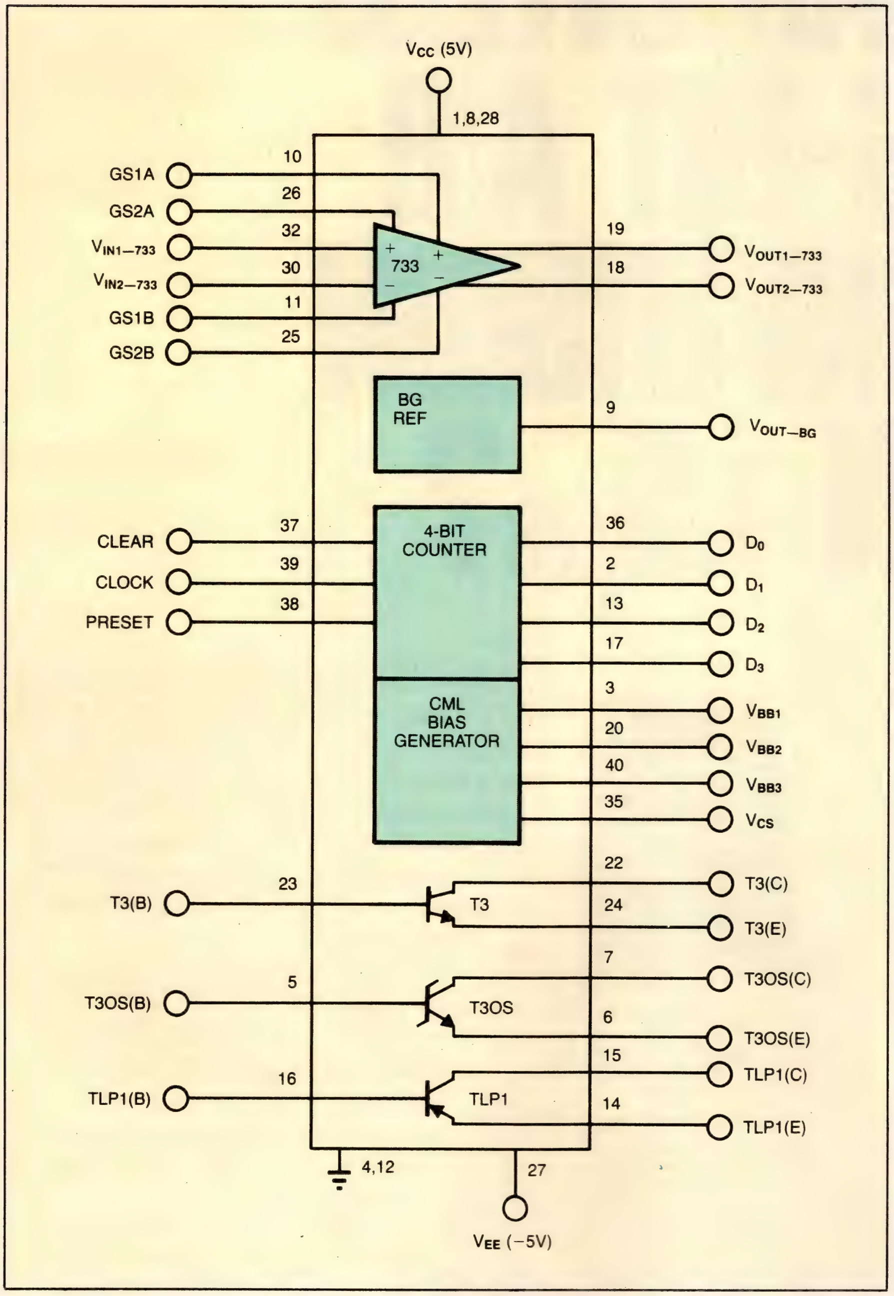


Fig 1—To evaluate the performance of its arrays, *VTC offers such evaluation chips as the VJ801. You have access to a 733-type op amp, a bandgap reference, a 4-bit counter, a current-mode-logic (CML) bias generator, and three transistors.*

ry 15%, so worst-case clock frequency should be 23 MHz (35 MHz÷1.30×1.15).

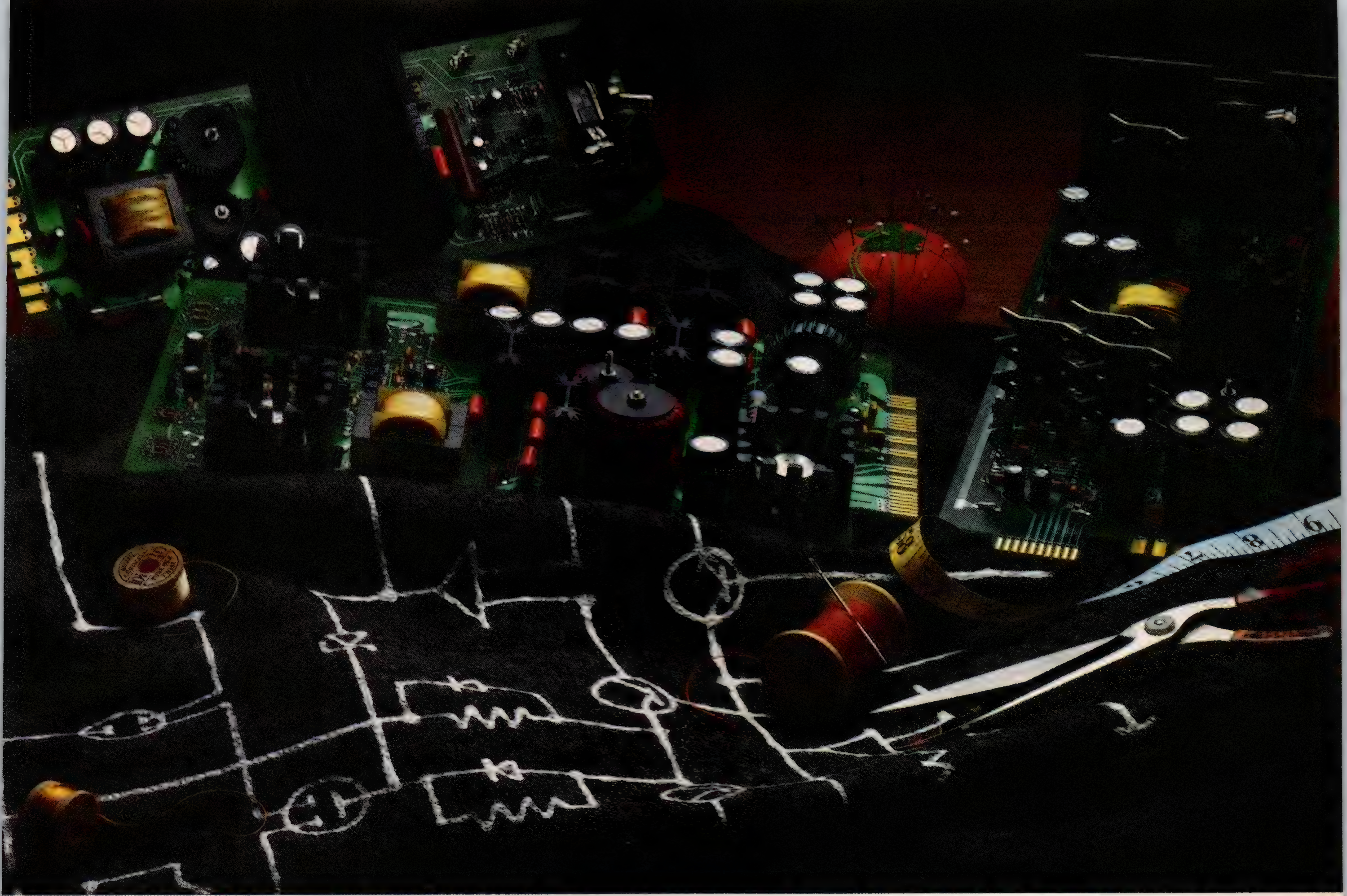
First bipolar standard cells

For higher-performance digital designs, you can use the first bipolar standard-cell library, the VL2000. Offered by VTC, it includes high-power cells that exhibit 440-psec internal gate delays, allowing clock rates as high as 500 MHz typ. The library includes such typical SSI and MSI cells as logic gates, registers, decoders, and multiplexers. The company is developing some higher-level cells like bit-slice ALUs and RAMs that should be available by March 1986. A/D and D/A converters should be available later in the year. Most cells have two power-speed versions; the high-speed version consumes three times the power of the low-power version but is twice as fast. For example, a D-type flip-flop in the high-speed version exhibits an 875-psec signal delay and dissipates 4.5 mW; the low-power version has a 1900-psec delay but dissipates only 1.5 mW.

Like the manufacturer's linear arrays, the VL2000 Series has a companion design system and evaluation chip to help you design your circuit. The VL2000 design system runs on a Mentor workstation and includes a logic simulator with delay calculations for logic and timing analysis. Unlike the case with arrays, the manufacturer performs layout. The evaluation chip, the VL2001, has two D-type flip-flops and two latches, one each of the high- and low-power versions. The chip has buffers to work with 10K ECL circuitry.

For VL2000-based designs, you calculate worst-case delay over process and temperature by multiplying your simulation results by the company's derating factors. Worst-case variation caused by processing requires a multiplication factor of 1.4; operation at 125°C derates the delay calculation by 1.25. For worst-case processing and temperature delay, you derate the results of your timing simulation by 1.73 (1.25×1.4). For military designs, therefore, the maximum clock rate that you could expect is 289 MHz (500 MHz÷1.73).

CMOS standard-cell ICs that meet military specifications are also available. Joining Hughes in this product area is NCR, which last September made its 3-μm CMOS II standard-cell library available for military-IC designers. The library has been available for commercial ICs through the company's Fort Collins, CO, facility since 1981. NCR's plant in Miamisburg, OH, which has produced military standard products, provides military processing for the library. The primary change in the library for military ICs is new worst-case parameters to take into account the wider temperature variation of the military ICs.



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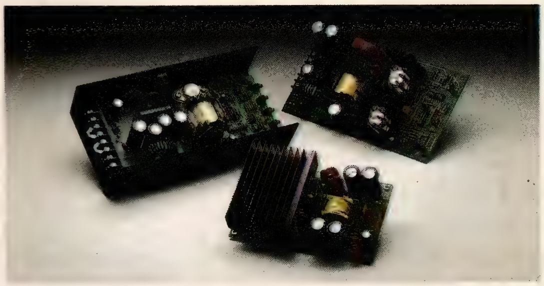

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For example, the library's RAM cell specs a maximum access time of 200 nsec for the commercial temperature range vs 225 to 250 nsec in the military range. The library has not been tested for radiation hardness.

More arrays supporting linear designs are becoming available for military systems. VTC offers its analog master chips, the VJ800, VJ830, and VJ860. The VJ800 is currently available, and the other two devices will be available by March. Each of the arrays is available with predesigned circuits so you can evaluate their performance (the evaluation chips have the designation VJXX1). For example, the VJ801 contains a 733-equivalent op amp, a bandgap voltage reference, a 4-bit current-mode-logic (CML) counter, a CML bias generator, a 0.5-mA npn transistor, an 8-mA Schottky npn transistor, and a lateral pnp transistor.

The op amp on the VJ801 compares favorably with standard op amps. It can provide three levels of gain—10, 100, or 300—depending on how you connect four gain-control pins on the IC. At the lowest gain setting (10), the op amp specs a typical bandwidth of 130 MHz when it drives a 15-pF load from a 50Ω source. At a gain of 300, the op amp shows a rise time of 7 nsec and propagation delay of 6.5 nsec. In comparison, Texas Instruments' μA733M military-temperature op amp specs a 10.5-nsec rise time and a propagation delay of 7.3 at a gain of 400. Therefore, the array's op amp delivers roughly the same ac performance as the Texas Instruments standard part. The standard part's CMRR is better than the semicustom part, however, at 86 vs 75 typ. **Fig 1** shows the VJ801 circuitry that you can use to evaluate the performance of the array. The device comes in a 40-pin side-brazed ceramic DIP, although the array is also available in plastic DIPs, flatpacks, tape-automated bonding packs, and plastic chip carriers.

The VJ800 array comprises 636 transistors, 706 resistors varying in value from 150Ω to 15 kΩ, 18 5-pF junction capacitors, and 40 bonding pads. The seven types of npn transistors on the array have a typical beta value of 100, f_T of 180 MHz, and current rating I_C between 0.5 and 180 mA. The 36 pnp transistors feature dual base contacts, 0.16-mA current rating, and a typical beta value of 120. The resistors include three types of diffused devices and two types of implanted devices. Absolute tolerance is 20%; for tighter tolerances, you can design circuits that depend on the ratio of resistances and take advantage of the 1% matching tolerance of the diffused resistors. (See **Ref 3** for a discussion of passive components in linear-array design.)

Two other arrays, the VJ830 and VJ860, provide transistors, resistors, and capacitors similar to those of the VJ800, but they are smaller arrays. They don't, however, include the 180-mA npn transistors. Each array has a corresponding evaluation chip (the VJ831 and VJ861) that allows you to test the on-chip components. Unlike the VJ801, these evaluation chips have no op amp or CML bias generator.

To design any of the VTC arrays, you purchase the vendor's design system for the particular array. These systems include data sheets for the arrays, a user's guide, a design manual, and a Mylar plot for laying out your chip. Also, you get component data so you can model the components for Spice simulation. The modeling information comes on a floppy disk compatible with Apollo workstations to use with the Mentor Graphics (Beaverton, OR) design workstations. Using the design system, you create a net list of your circuit and evaluate it using Spice. Notes in

For more information . . .

For more information on the semicustom ICs described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Applied Micro Circuits Corp
5502 Oberlin Dr
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(619) 450-9333
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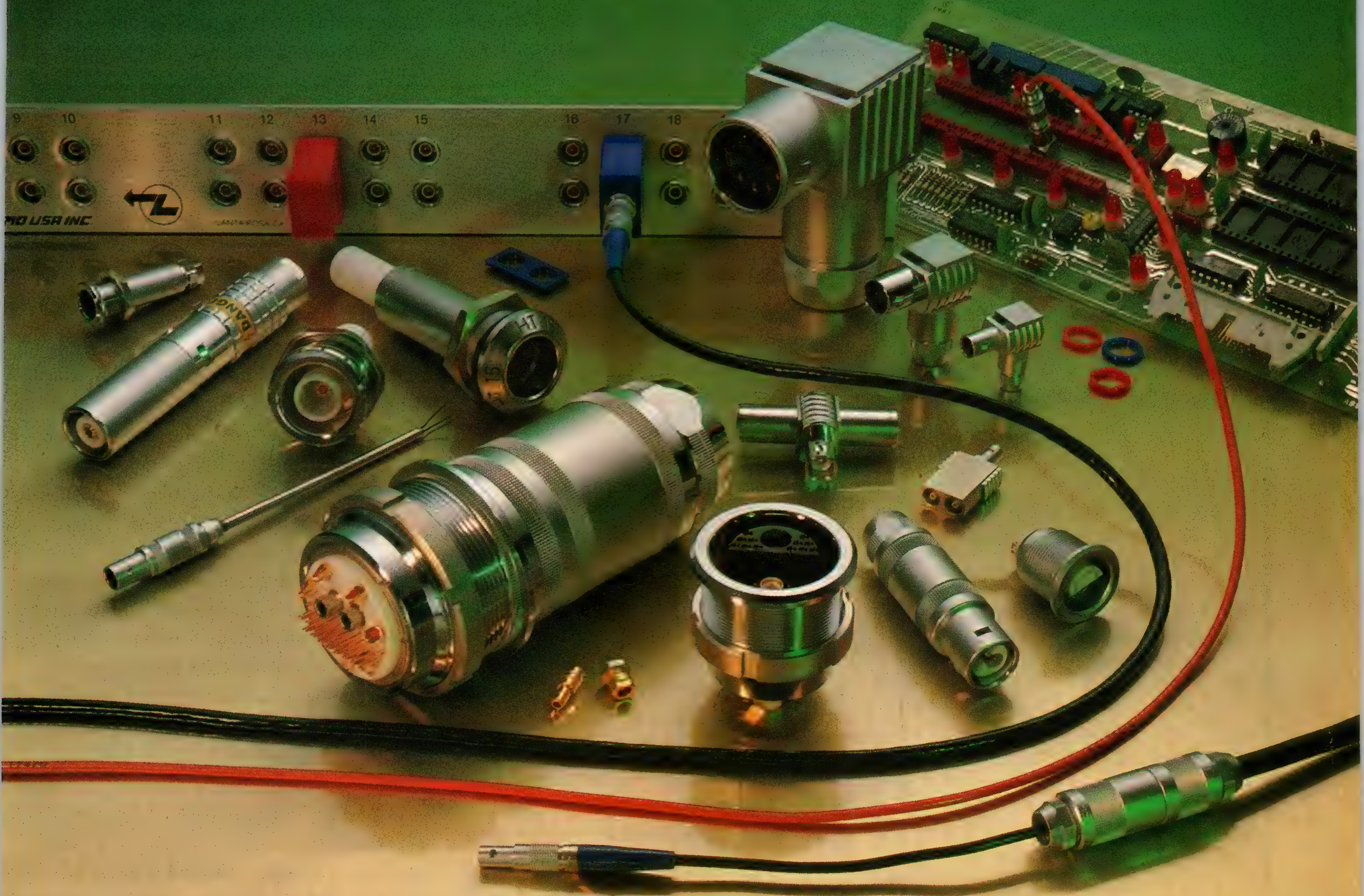

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the design system explain linear-array design methods, and the manual covers such topics as parasitic impedances, I/O-port circuits, and gauging reliability. Once you're satisfied with the net-list simulations, you can lay out the chip on Mylar or have VTC do it for you.

Macrocells make op amps

Raytheon offers MIL-STD-883C processing for its RLA120 linear macrocell array. This array differs from the previous arrays because, in addition to uncommitted transistors and resistors, the RLA120 contains 12 macrocell gain blocks. Raytheon provides a layout that converts any of the gain blocks into either an op amp (4558-, 324-, or 3403-type) or a voltage comparator (339- or 365-type). The layout that customizes the gain blocks uses the same metal mask that defines your interconnection pattern, so you determine the function of each gain block and interconnect the blocks with the other components in the array.

The company supplies three evaluation chips with the macrocell gain blocks specified and connected to pins so you can evaluate array performance. The 4558-type op amps spec a unity-gain bandwidth as high as 20 MHz; the maximum input offset voltage over military temperatures does not exceed 6 mV. Both the CMRR and PSRR exceed 70, and the output voltage can swing between −10 and +10V min if you use ±15V power supplies. The evaluation chips come in 16-pin DIPs, but Raytheon offers a choice of plastic or ceramic DIPs and leadless chip carriers that have between 14 and 24 pins.

Tektronix, which entered the linear-array market last May, can process its three bipolar arrays to military standards. These arrays, called Quickchips, feature npn transistors with a typical f_T of 6.5 GHz, the fastest silicon-array transistors available. Quickchip 1 contains 18 transistors and 13 resistors, so it is useful for implementing small designs. Quickchips 2 and 3 offer hundreds of transistors and resistors and employ a cell-based architecture that simplifies the design of more complicated linear devices. Quickchip 3 does not include the 6.5-GHz transistors found on Quickchips 1 and 2, but it contains high-voltage transistors that spec a collector-base breakdown voltage (BV_{CBO}) of 65V and a collector-substrate breakdown voltage (BV_{CS}) of 95V min.

In general, where the commercial semicustom-IC market goes, so goes the military (eventually). The trend toward higher integration and automation is leading many commercial semicustom-IC companies into silicon-compiler approaches, and military-IC companies are following. Along these lines, Silicon Compilers Inc (San Jose, CA) has entered into agreements with two military-IC manufacturers to hasten the development of military-specified processes that can fabricate designs created with Silicon Compilers' tools. Honeywell has provided design rules for its CMOS III processsing technology for Silicon Compilers' Genesil design system, and the companies will design and fabricate a test chip to verify its performance. Silicon Compilers has also entered into an agreement with General Dynamics (St Louis, MO) to further the compiler company's experience in the design of military ICs. **EDN**

References

1. Integrated Circuit Engineering Corp, "Hi-Rel Semiconductors," Icecap Report, Issue 3-9, 1983.
2. Smith, David, "Gallium arsenide challenges silicon in high-speed array applications," EDN, June 27, 1985, pg 75.
3. Ritmanich, Will, "Understand the limits of passive analog IC components," EDN, October 17, 1985, pg 155.

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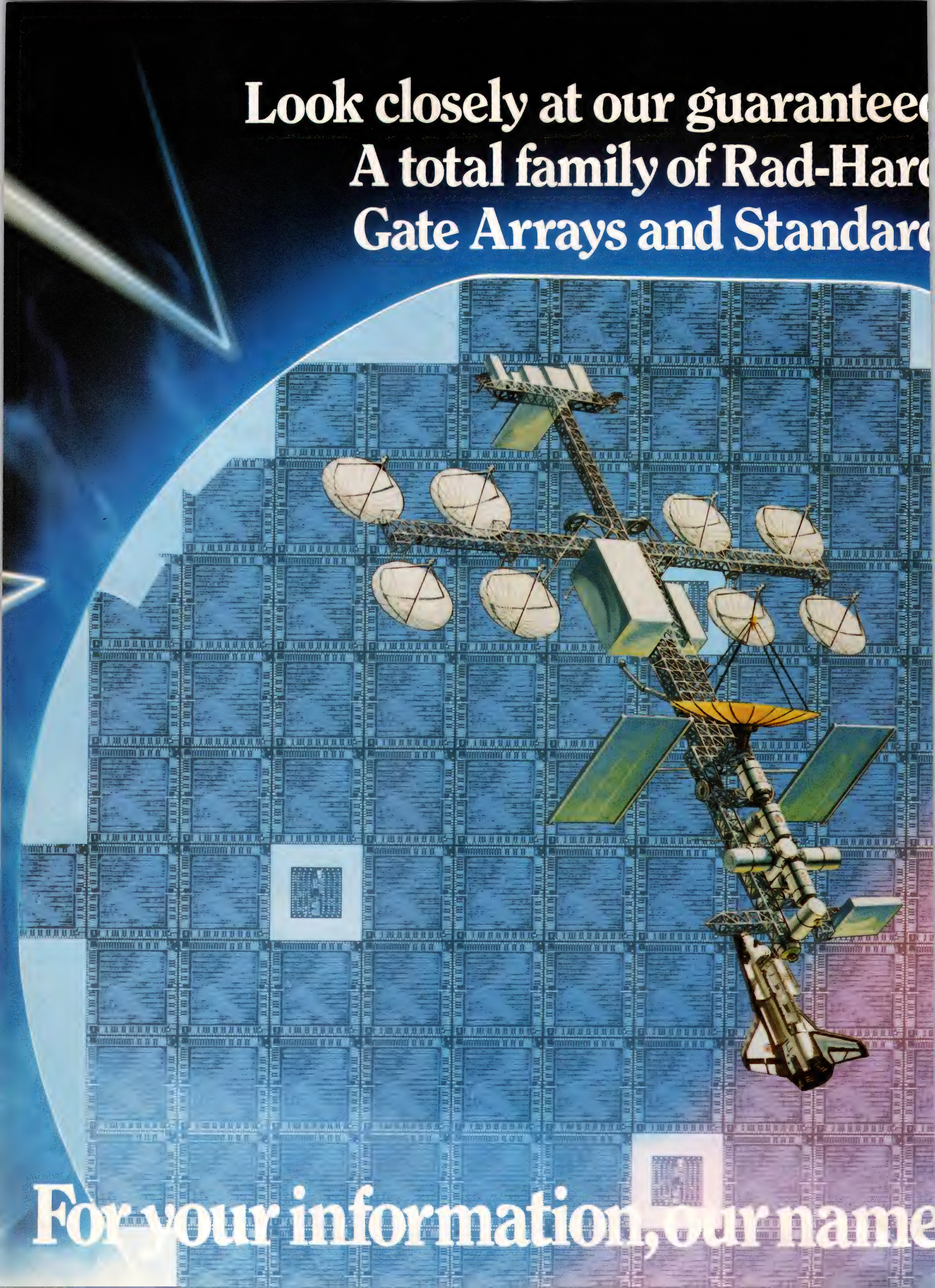

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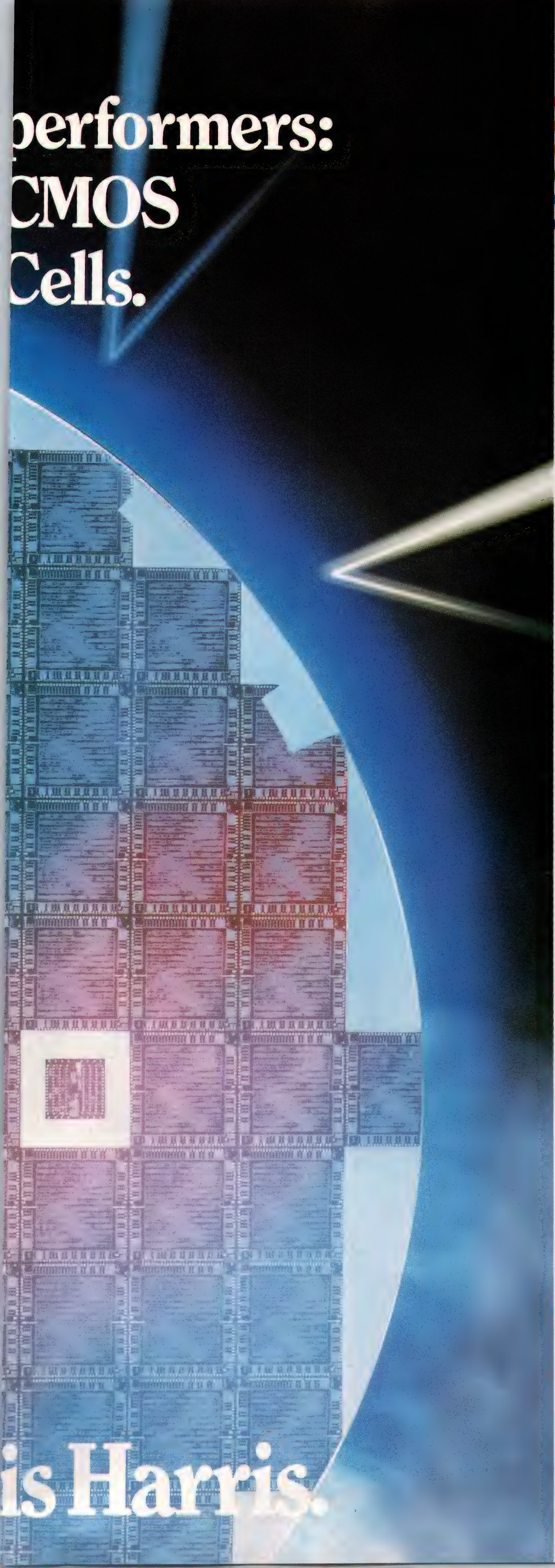

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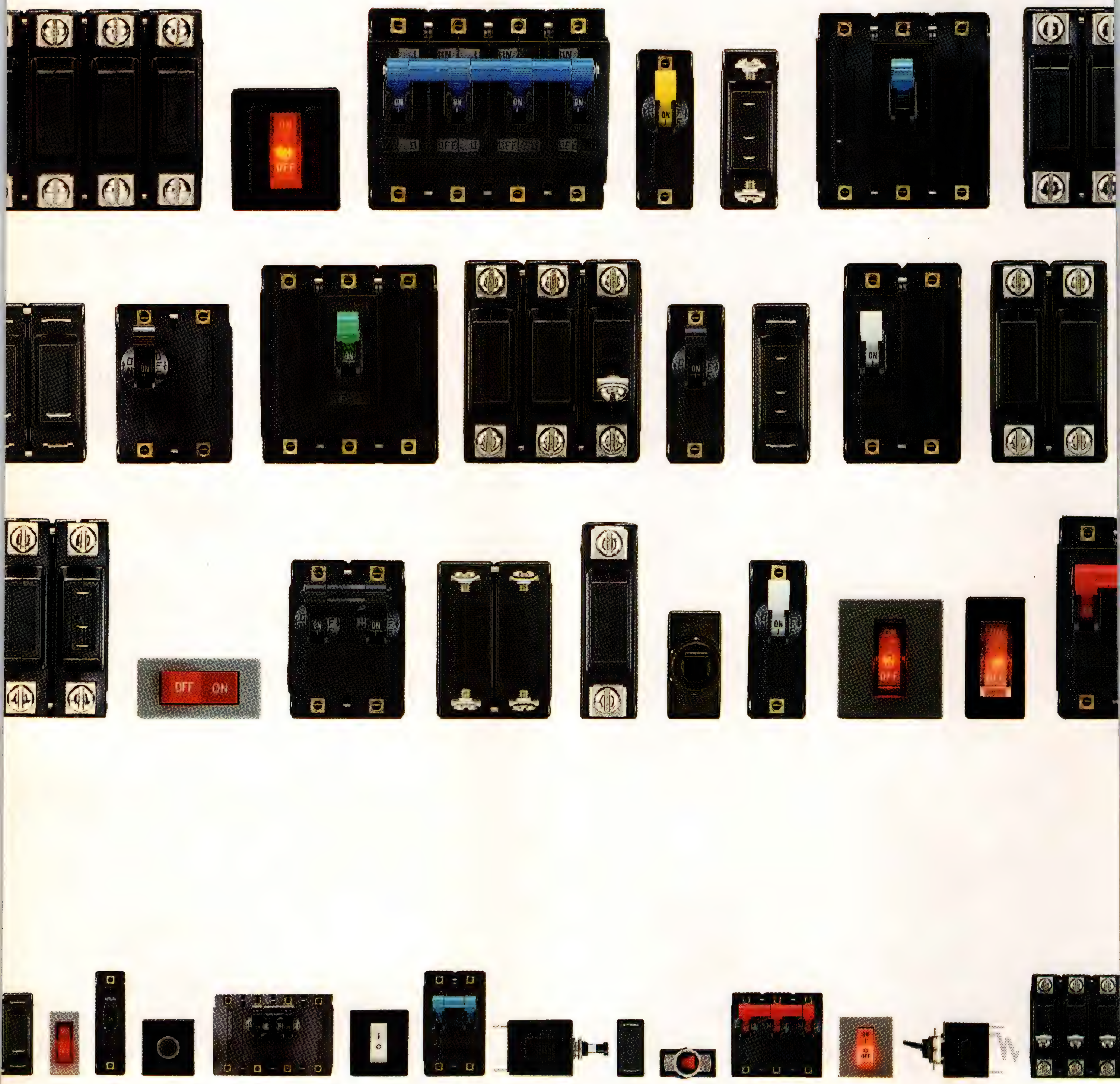

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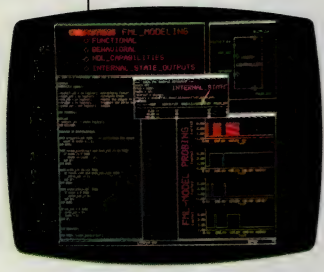

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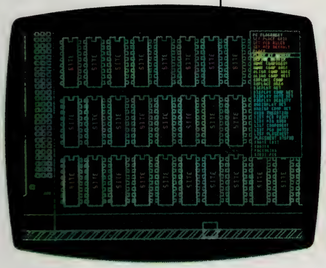

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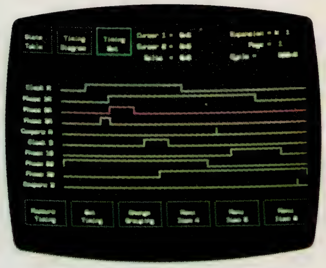

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CIRCLE NO 169

Ruggedized IBM PCs and compatibles serve in low-cost industrial systems

Chris Terry, *Associate Editor*

If you're designing a compact computer system for use in harsh industrial environments, consider basing your system on the IBM PC/XT, PC/AT, or a compatible machine or CPU board. You can design a PC-based system that can handle almost any application that an industrial system based on a minicomputer—such as the DEC LSI-11—can handle, but at roughly half the cost of a minicomputer system. Moreover, software for PC-based systems is relatively inexpensive, and system-development time can be relatively short.

Prices for industrial Multibus-, VME Bus-, and Q Bus-board computers start at approximately $20,000. By comparison, an industrial PC costs approximately $12,500. And although these more-expensive Multibus-, VME Bus-, and Q Bus-board computers are designed specifically for industrial use, you may still have to put them into NEMA enclosures before you can use them on the factory floor.

To operate in very harsh industrial environments—for instance, in the presence of vibration or dust, or in a corrosive atmosphere—a PC-based system will also need a NEMA enclosure, but an enclosure for a PC will be much smaller and less expensive than one for a minicomputer.

Bubble memory can replace disk storage *in the Amdex RPC-50, a rugged industrial computer that's compatible with the IBM PC/XT.*

Only a few vendors—such as IBM, Amdex Corp, and Sigmation —supply complete industrial microcomputer systems. IBM offers the 5531 and 7531, which are industrial versions of the PC/XT and PC/AT. Both computers are housed in heavy steel enclosures. Each system includes a filter, a cooling fan, a thermal sensor for overtemperature shutdown, a locking door for the disk drives, and an internal retainer that holds plug-in cards in place. The keyboard is protected by a Mylar membrane, and the monitor screen has a plastic cover.

The computers operate over 4 to 41°C and withstand 8 to 80% noncondensing humidity. They tolerate vibration of 0.07g at 17 to 200 Hz and 0.035g from 200 to 500 Hz, and they can withstand 0.5g shock for 10 msec. With 256k bytes of RAM, a 10M-byte hard disk, and a color monitor, the 5531 costs $6779. With 512k bytes of RAM, a 20M-byte hard disk, and a color monitor, the 7531 costs $8994. The 7532, a rack-mount version of the 7531, costs $9860 and comes with the necessary rack-mounting hardware.

Although the 5531 and 7531 are suitable for many heavy-duty applications requiring continuous use of the computer (eg, climate control in

1240 and 1630 were fine,

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Trigger Levels	14	5	15
Memory Depth	2K	1K	4K
State/Timing Correlation/ Display	No	No	Yes
Timing Logic Analysis	Yes	Yes	Yes
Acquisition Speed	100MHz	100MHz	100MHz
Channels	18	8	16
Transitional Timing	No	No	Yes
Pattern Generation	No	No	Yes
Channels	–	–	160
Speed	–	–	20MHz
Vector Depth	–	–	8K
Software Analysis	assembly only	assembly only	high-level and assembly
Symbolic Trace	No	No	Yes
Performance Analysis	statistical	statistical	real-time non-statistical
Code Coverage	No	No	Yes

1240 includes 2-1240D1 & 2-1240D2 - 1630G includes 57 state/8 timing
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large buildings), they may not be rugged enough for a really harsh environment such as a factory floor, where the atmosphere may be contaminated with dust and metal particles, and where the computer's case could be splashed with water and oil. To use these computers in such an environment, you'll have to put them into NEMA enclosures.

Other vendors offer IBM PC-compatible systems that have greater tolerance of temperature, humidity, vibration, and shock. The PC/XT-compatible RPC-50 from Amdex, for instance, is much more rugged than the 5531, although it doesn't offer as much storage as the IBM machine does. The RPC-50 operates over 0 to 55°C and withstands 5 to 95% noncondensing humidity.

The system is housed in a heavy steel case that's sealed against liquids other than oil. The case also has pressurized cooling, which protects the unit from dust. To protect the computer from oil, you could enclose the case in a standard NEMA-4 or NEMA-12 cabinet.

You can choose bubble-memory or hard-disk mass storage for the RPC-50. The hard-disk drive can tolerate 1g vibration along any axis from 10 to 350 Hz, and it can withstand shocks of 10g for 8 msec. Because it has no moving parts, the bubble memory has even greater tolerance of vibration and shock. With 128k bytes of RAM, one serial port, and 128k bytes of bubble-memory mass storage, the RPC-50 costs $3450; with a 10M-byte hard disk, it costs $3990. For $95, you can add 256k bytes of RAM. You can obtain as much as 1M byte of bubble memory (for an additional $3970), but the vendor must install it at the factory.

Another complete system, the BC-12 industrial computer from Action Instruments, provides hardware and software compatibility with the IBM PC/XT. The system is modular in construction and is based on a passive PC bus. Housed in a wall-mounting NEMA-1 enclosure, each board has a protective metal shroud that's bolted to the frame to prevent displacement of the board by vibration or shock. The system comes with 256k bytes of RAM on the 8088 CPU board and has seven expansion slots for additional memory and peripheral interface boards.

The complete unit fits into any standard NEMA enclosure. The system operates over 0 to 55°C and in noncondensing relative humidity of 0 to 90%. The hard-disk version withstands continuous vibration of 0.5g; the bubble-memory version can tolerate 2.5g vibration. An optional 512k-byte bubble-memory module plugs into the system bus. Including the chassis, power supply, 8088 CPU/memory module, and a multifunction module with one serial and one parallel port, the BC-12 costs $2995.

Rugged mother boards

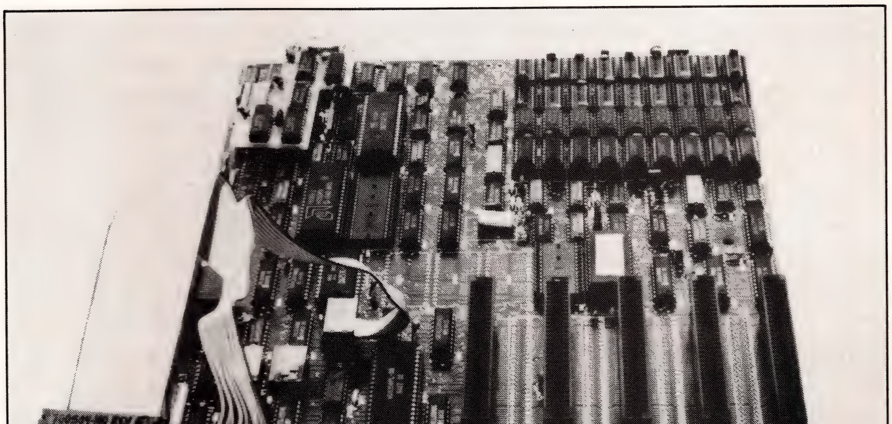
Although developing your system around a complete industrial PC may get your product to market quickly, developing your system around a rugged CPU board will give you more flexibility in configuring your system. You can start with a rugged mother board like Sigmation's IBM PC/XT-compatible Turbo/XT or IBM PC/AT-compatible XT286, for example. The Turbo/XT includes 64k bytes of RAM that's expandable to 1M byte and a 16-bit 8088 CPU that can address as much as 840k bytes of additional memory. The mother board supports an optional 8087 numeric coprocessor.

The Turbo/XT's CPU operates at 8 or 4.77 MHz. The board has eight I/O expansion slots that support such boards as disk controllers, multifunction boards, local-area-network controllers, monitor controllers, and modems. Three DMA channels on the I/O bus support high-speed transfers directly between the I/O devices and memory. The XT286, which runs at 6 or 8 MHz, has six I/O expansion slots.

Both boards operate over 0 to 50°C and withstand noncondensing humidity of 0 to 95%. They tolerate 0.07g vibration at 5 to 500 Hz and 0.5g shock for 10 msec max. With 704k bytes of RAM, the Turbo/XT costs $449 (100). The vendor also offers complete industrial systems based on these boards.

The passive-mother-board scheme

For even more flexibility in configuring your system, consider using the passive-mother-board scheme, in which the mother board acts merely as a passive bus, while



You can build a compact industrial system *around an IBM PC-compatible mother board like the Turbo from Sigmation. The Turbo includes an onboard, parallel printer interface; an asynchronous line interface; and support for a hard-disk drive.*

Offering 50,000 12-bit A/D conversions per second, *MetraByte's 16-channel data-acquisition board is compatible with the IBM PC/XT and PC/AT. The DASH-16 board performs all data transfers to the CPU in DMA mode.*

the active circuitry (CPU, memory, I/O interfaces) resides entirely on plug-in boards.

The passive-mother-board configuration has several advantages. First, it makes system maintenance much easier—instead of dismantling the system to get at the mother board, you merely replace a board or two. And then, the scheme lets you upgrade an existing system merely by substituting a faster CPU board or adding a peripheral-interface board. To upgrade a standard PC unit, for example, you could add an accelerator board containing a fast CPU—such as an 80186, 80286, or 68000—which performs the main processing tasks while offloading I/O tasks to the original 8088 CPU.

Another benefit of the passive-mother-board arrangement is that you can easily obtain CPU boards that offer more protection against high temperatures, humidity, vibration, and shock than the IBM PC mother board offers. Vendors such as Faraday, Action Instruments, Gould Inc, and Amdex Corp offer CPU, memory, and interface boards that have specified operating ranges of 0 to 60°C and 5 to 95% relative (noncondensing) humidity and that withstand shock and vibration better than do boards designed for commercial environments.

Further, if you use the passive-mother-board scheme with state-of-the-art VLSI chips, you can build a system that's much more compact than a standard PC, yet still fully compatible with the IBM machine. Faraday, for example, offers a PC/XT-equivalent CPU on the Bus PC/256, a half-size board with a 2-chip set of CMOS gate arrays that provides all of the CPU support circuitry. The board costs $695. The company's Bus AT/512 puts a PC/AT-equivalent CPU on a full-size card. The Bus AT/512 comes in two versions: a 6-MHz model ($1295) and an 8-MHz model ($1395).

Basing your system on a PC or compatible machine will give you a wide choice of plug-in peripheral controllers as well. Plug-in boards for controlling such standard equipment as terminals, printers, and D/A and A/D converters are readily available from many vendors at a relatively low price.

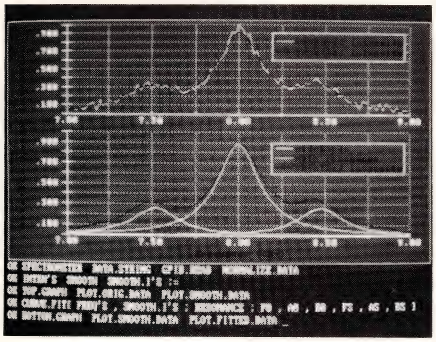
A board with two serial ports and a parallel port, for instance, may cost $200 to $300 for the PC bus. A similar board for the Multibus or VME Bus could cost as much as $450 to $650. Among the interface boards for the PC are Amdex's industrial-grade multifunction card, which costs $335. MetraByte's 8-channel A/D converter card with 12-bit resolution costs $395; the company's 16-channel A/D converter with DMA data transfer sells for $945.

Plug-in interface boards

Data Translation's DT801 Series boards provide as many as 16 A/D converter channels with 12- or 16-bit resolution and sampling rates as high as 27,500 samples/sec. The DT2801 board costs $995. Another board, MetraByte's Dash-16 16-channel A/D interface board, can handle as many as 4000 conversions/sec using interrupt-driven or programmed transfer to an array variable. The Dash-16 can handle as many as 50,000 conversions/sec using DMA transfer; it costs $945.

If your system will include more exotic peripherals—such as gas chromatographs or liquid-flow instrumentation—you may need to design a custom interface board. Your task will probably not be difficult: IBM's PC bus, which provides a standard hardware interface, is considerably simpler and less expensive than Multibus, VME Bus, or Q Bus. In addition, the company has published full details of the bus and of the operating system, PC-DOS, which provides a standard software interface. So, whether you obtain peripheral-controller boards from a vendor or build your own, the boards will cost less than comparable boards for minicomputer-based industrial systems.

These industrial peripheral-controller boards may even eliminate the problem of obtaining industrial shielding for your computer. When you use plug-in boards to control peripherals in an industrial environ-



***You can analyze and display instrumentation data** with the aid of MetraByte's Asyst scientific software package.*

ment, you can put the actual computer in a remote location and run shielded cables to the peripherals. This scheme would give you even more flexibility in developing your system and cut costs even further. In fact, you wouldn't have to use an industrial PC in your system; you could use any PC that could perform the necessary functions for your purposes. You could, therefore, use a standard PC/XT or PC/AT located in an office environment and house only the remote units in NEMA enclosures.

Remotely locatable boards

Among the remotely locatable boards available for the PC bus are MetraByte's expansion multiplexers (the EXP-16 costs $365) and solid-state, optically isolated I/O control boards (the SRA-01, with 9 input or output modules, sells for $271). These boards communicate with the PC via a ribbon cable and a common interface board that plugs into a slot on the PC mother board. The boards operate over 0 to 50°C and withstand noncondensing relative humidity of 0 to 90%. The pc boards are thicker and use heavier traces than common pc boards. Further, because they're clamped to the mother board, they withstand shock and vibration conditions of the magnitude likely to be encountered in a manufacturing environment.

Other vendors, such as Action Instruments, supply similar interface boards, as well as microcomputers for controlling and processing input and output signals. These boards communicate over an RS-422 link with a standard IBM PC/XT or PC/AT located in an office environment. The computer performs overall control and analyzes incoming data.

Whether your application calls for custom software or software that you can buy off the shelf, you'll probably pay less for programs written for a PC-based system than for software that's written for another, more complex, system.

Software for your system

Vendors of both plug-in and remotely locatable interface boards supply software that, at the very least, allows the IBM PC to capture incoming data and store it on disk. Many vendors also supply analytical routines as part of the package. Depending on the application, these routines may include digital-signal-processing algorithms (such as FIR, IIR, and FFT), statistical algorithms, or graphics routines for the display of recorded or real-time data.

MetraByte's Labtech Notebook software ($895), for example, allows you to set up all the parameters for a data-acquisition run, with different sampling rates and scaling for each A/D converter channel. You don't have to have any programming skills to use Labtech Notebook; you simply reply to software prompts, which elicit all the necessary information. You can save your replies in a command file that the program can use in future runs.

MetraByte offers a $1695 version of Macmillan Software's Asyst package for the Dash-16 board. The package supplies such analytical routines as polynomial mathematics and evaluation, vectors and matrices, solutions to simultaneous equations, fast Fourier transforms, and least-squares approximations. The Unkelscope package ($595), also from MetraByte, is designed for use with the company's analog interface boards; it emulates an oscilloscope, chart recorder, or X-Y plotter and comes with digital filtering, integration, and differentiation routines. A number of other interface-board vendors make boards that are compatible with Labtech Notebook.

Because your system will be IBM PC compatible, however, you won't be limited to using your vendor's proprietary analysis package. Instead, you can use any spreadsheet or data-analysis program that runs on the IBM PC.

Because the hardware and software interfaces for PC-compatible machines are standard and simple,

For more information . . .

For more information on the IBM PC-compatible systems and software described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

Action Instruments Inc
8601 Aero Dr
San Diego, CA 92123
(619) 279-5726
Circle No 718

Amdex Corp
16 Woodhaven Dr
Andover, MA 01810
(617) 470-0561
Circle No 719

Data Translation Inc
100 Locke Dr
Marlboro, MA 01752
(617) 481-3700
Circle No 720

Faraday Electronics
743 Pastoria Ave
Sunnyvale, CA 94086
(408) 749-1900
Circle No 721

Gould Inc
Haverhill St
Andover, MA 01810
(617) 475-4700
Circle No 722

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Manufacturing Systems Products
Box 1328
Boca Raton, FL 33432
Phone local office
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Stoughton, MA 02072
(617) 344-1990
Circle No 724

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Sigma Information Systems
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Anaheim, CA 92806
(714) 632-0474
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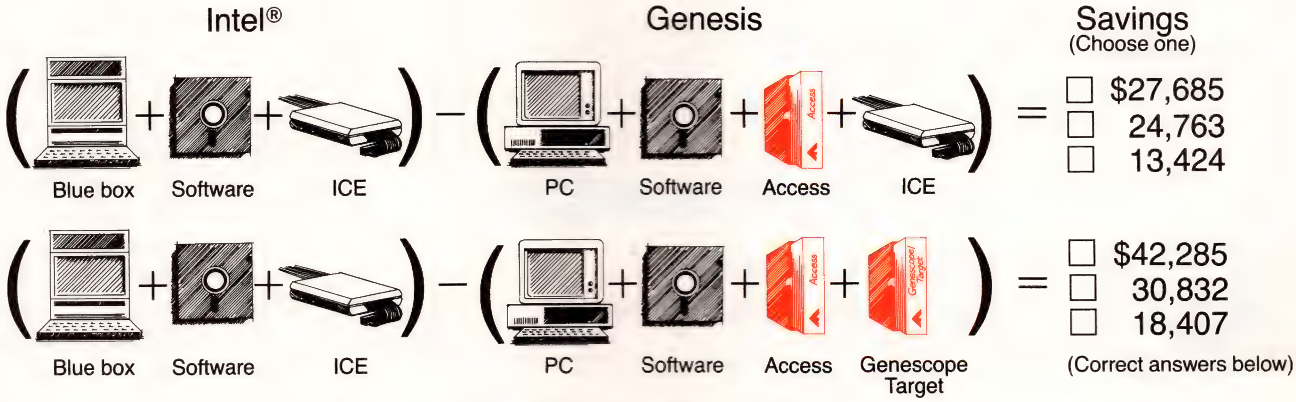
The new 8086 arithmetic:

(Test yourself)



Thanks to Genesis' ACCESS™ 86 software, you can save thousands of dollars on the cost of each development system. And you'll save a fortune in time to boot. With ACCESS 86, Intel software runs on an IBM® PC, XT or AT,™ using MS-DOS. And runs far better than it ever did on Intel's machines.

Choose any language—PLM/86, Fortran, Pascal or our special implementation of Mark Williams C. ACCESS 86 supports all the Intel locating and linking utilities. If you already have the Intel software, just download it into your PC. If you don't, it's available directly from Genesis. ACCESS includes software to transfer files back and forth.

New 8-bit capability Besides the 8086 family of chips, Genesis now offers ACCESS II for Intel's ISIS development software. With a single card or replacement chip in your PC, ACCESS II lets you run Intel 8080 software and utilities at about four times the speed of an MDS-230.

Several times as fast Depending on your hardware, you'll compile and link programs up to eleven times as fast as with an Intel system. And that's only one way you'll save time.

Superior debugging Genescope™ is a full-screen symbolic debugger for programs written in any of Intel's languages. You can window source or listing files during a session, scroll through trace and memory, and make patches with an on-line symbolic assembler. Step through code line by line on the screen. High level line numbers and symbols are available as you debug. Some users report they're completing projects in one-third the time.

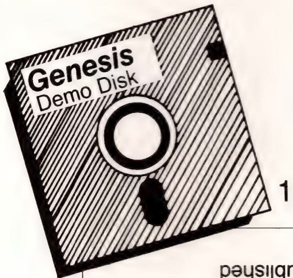
A version of GeneScope is available for debugging with the most popular emulators. It has the same easy interface.

But maybe you won't need an emulator at all.

In-circuit testing without an emulator Genescope/Target™ lets you download your program into the target system and debug it there. You get most of the features of an emulator at about one-tenth the cost.

Free demo disk Genesis will be happy to mail you a disk that shows how this slick little system works. Slip it into your PC and find out why more than 1,000 developers have switched to Genesis development tools. To get your copy, just pick up the phone and call:

(415) 964-9001



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Correct answers: With an emulator: $27,685. Without an emulator: $42,285. Incredible but true! These figures are based on Genesis' published prices and quotes from Intel.

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CIRCLE NO 49

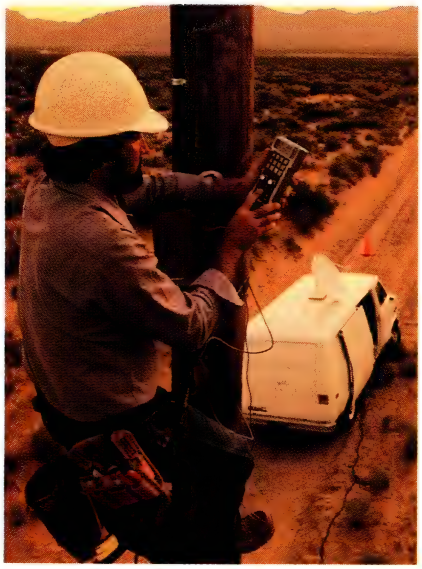
you can put together a PC-based industrial system quickly and easily. In fact, you can probably get your PC-based system up and running in half the time it would take to get a minicomputer-based system up and running.

For one thing, you can develop both hardware interfaces and software on a standard PC, which will, of course, closely resemble your system in both architecture and configuration. In contrast, you must often do such development for a Multibus or VME Bus system, on a very different machine with the aid of emulators and cross compilers. Systems based on the Multibus or VME Bus generally require extensive engineering support at the site level, and they need much more user support than do systems based on the PC bus. Thus, OEMs can bring a new PC-based system to market much more quickly than they could get a Multibus- or VME Bus-based system to market. **EDN**

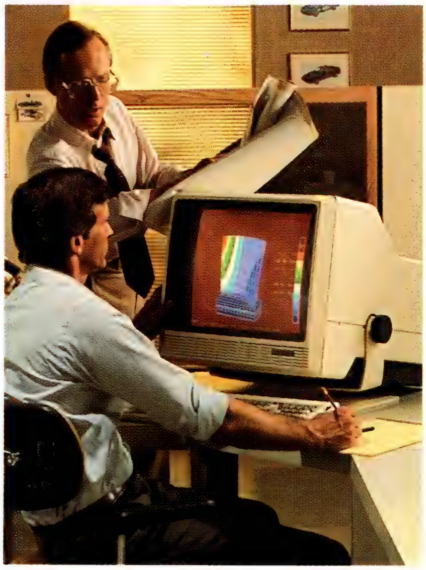
Article Interest Quotient
(Circle One)
High 503 Medium 504 Low 505

New superfast signal processor from Texas Instruments keeps transactions strictly private...

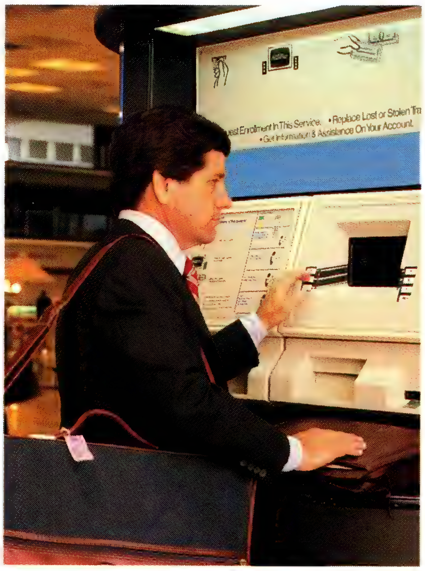
strengthens signals, enhances squelches echoes, and gets you Meet TI's new TMS32020



Echo cancellation can be greatly improved by using new TMS32020 processor, allowing telephone messages to come through loud and clear from anywhere.



Graphics systems could be economically implemented with TI's TMS32020 supplying throughput capability required for realtime rotation, scaling, and translation.



High-speed modems (4.8K bps to 19.2K bps) can be built with fewer chips and in shorter development time using TI's new TMS32020 processor.

It can handle all your digital signal processing (DSP) better than ever before. And as you will read, TI's new, single-chip TMS32020 can also be an efficient, economical processor for many high-speed, numeric-intensive applications.

And because it is available now, fully supported, the TMS32020 can speed your system development.

Up to three times faster throughput

TI's new TMS32020 processor delivers two to three times the throughput of the industry standard, TI's own TMS32010.

Behind this dramatic increase are (1) an expanded instruction set with repeat feature, (2) an expanded memory capability both on chip and off, and (3) much faster I/O.

Top secrets stay top secret when secure-telephony systems (on cover) are designed using TI's new TMS32020 signal processor. Its vastly improved throughput allows it to perform all critical subroutines so rapidly that deciphering the code is made virtually impossible.

Like the TMS32010, the TMS32020 utilizes a modified Harvard architecture emphasizing overall system throughput, communication, and flexibility in processor configuration.

Increased capability and flexibility

Having greater throughput, TI's TMS32020 makes fast work of filtering, correlation, windowing, transforms, wave-form generation, and all your other DSP tasks. 544 words of on-chip RAM, 32-bit arithmetic, single-cycle multiply/accumulate instructions, and an independent auxiliary register arithmetic unit further equip the TMS32020 for realtime DSP systems.

However, the capabilities of the TMS32020 should challenge your imagination. Its 64K word program *and* 64K data-memory spaces, timer, serial port, multiple-interrupt structure, provision for external wait states, and multiprocessor interface capability make the TMS32020 a natural choice for wide use.

And the TMS32020 is economical. Through VLSI implementation, the TMS32020 incorporates all these features into a single, 68-pin grid-array package.

Full support shortens development time

A wide range of development hardware and software tools is available to shorten your design cycle. Included are full-speed emulators, software simulators and assemblers/ linkers, and application reports, plus other documentation (*see box*).

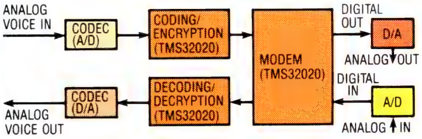
Three-day DSP workshops are conducted periodically at TI's Regional Technology Centers, and TI application engineers are also ready to provide help. Extensive third-party support is available.

A TMS32020 applications handbook and additional documentation are only 11 quick keystrokes away, 1-800-232-3200, ext. 3502, or use the coupon on page 4.

Where economy is a prime design consideration and system requirements are less demanding, use TI's industry-standard TMS32010 DSP. An extended temperature range military version is also available.

graphics,
to market faster.
digital signal processor chip.

TMS32020 provides all secure-telephony features



Because it can perform several functions by simply executing a variety of subroutines, TI's TMS32020 processor is a prime candidate for secure-telephony applications.

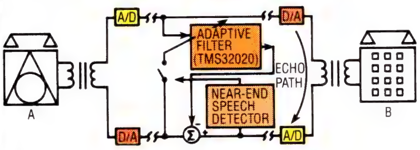
For example, multiple TMS32020s can compress the voice, encrypt the digital signals, and act as a modem.

The fast cycle time of the TMS32020 is not only essential to the encryption/decryption routine but can also allow the routine to be constantly varied so that cracking the code would be difficult.

The large program memory, serial port, and single-cycle multiply/accumulate facilitate the coding, decoding, and modem routines.

Thus, the TMS32020 is an effective alternative to the costly fully custom circuits you would have to use to gain equivalent processing power.

TMS32020 cancels echoes more accurately

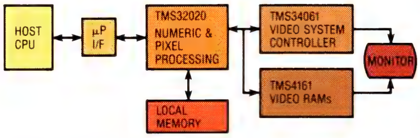


For more effective echo cancellation, the 544-word on-chip data memory of TI's TMS32020 enables it to provide larger, more accurate adaptive filters. Because of this memory and the single-cycle multiply/accumulate/data move, the TMS32020 can execute and update a 128-tap adaptive filter needed by the echo-cancellation-model routine. And the extraordinary speed of the TMS32020 allows the adaption routine to execute in real time.

The TMS32020 completes a multiply/accumulate/data move in a single cycle. Its "repeat instruction" allows the next instruction to be repeated "N" times, which saves program memory space and effectively pipelines the instruction.

In addition, the 544 words of on-chip data RAM allow quick updates of taps for faster adaptation, and the serial I/O port allows direct interface to a codec with little or no "glue" logic.

TMS32020 excels at fast matrix manipulations



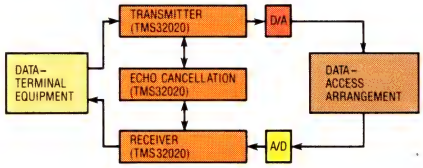
In graphics applications, TI's TMS32020 processor can be used for both numeric and pixel processing. Its 200-ns multiply/accumulate allows the TMS32020 to execute realtime graphics scaling, rotation, and translation. All depend upon memory-intensive matrix manipulations that require rapid execution.

The block-move feature of TI's TMS32020 — up to 80 Mbits per second — allows the large data blocks involved to be accessed in real time to manipulate the screen. The TMS32020 is capable of addressing up to 64K 16-bit words of data used to store the pixel information. Among other features that give the TMS32020 an edge in graphics systems are the scaling shifter used in pixel or bit alignment and the wait states that allow communication with slower DRAMs/VRAMs.

Because a graphics system must interface to a host processor, the host-interface logic on the TMS32020 eases your design task.

TMS32020 simplifies high-speed modem design

Using multiple TMS32020 processors in high-speed modems is a logical choice over costly fully custom chips. The TMS32020 combines easy programming with large data memory, multiprocessor and



serial interfaces, overflow mode, large program memory, and table access of program memory.

Since many high-speed modems require more than one programmable DSP chip, the built-in multiprocessing interface of the TMS32020 minimizes component count and simplifies design.

Adaptive FIR filters require the single-cycle multiply/accumulate/data move and the large data memory of the TMS32020 for high-speed computations and realtime implementation.

The overflow-saturation mode minimizes errors caused by an overflowing accumulator and produces a "clean filter."

Program memory of up to 64K words permits multiple bit rates and standards to be supported simply in software rather than hardware.

For more applications data, call 1-800-232-3200, ext. 3502, or check the coupon on page 4.

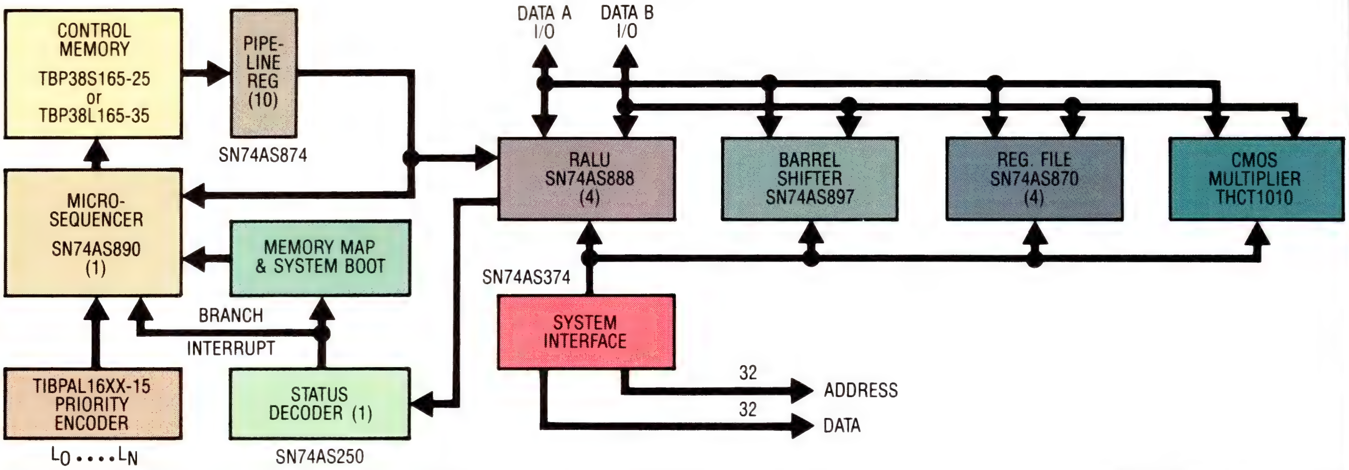
Samples of TI's new 32020 are available now through authorized TI distributors, at $250.* Volume production is slated for early 1986. Development-support tools are also available off the shelf.

TMS32020 Software and Hardware Support

Host Computer	Operating System	Part Number
Macro Assembler/Linkers		
DEC VAX	VMS	TMDS3241210-08
TI/IBM PC	MS-DOS	TMDS3241810-02
Simulators		
DEC VAX	VMS	TMDS3241211-08
TI/IBM PC	MS-DOS	TMDS3241811-02
Hardware		
Emulator		TMDS3262220

*Suggested retail, quantity 1, U.S.A.

Turn the page for more information.



High system performance and low-power operation result when four of TI's new 74AS888 8-bit-slice processors are cascaded to form a 32-bit CPU with TI's new, low-power THCT1010 speeding multiplier/accumulator operations.

TI redefines your idea of speed/power ratios with its new bit-slice/multiplier team.

For many applications requiring exceptional system execution speeds, TI's new 74AS888 8-bit-slice processor can prove the effective alternative to the TMS32020 DSP.

Usually, when you increase system performance significantly, power consumption follows right behind — just as night follows day.

Not so with TI's IMPACT™ 74AS888 and new THCT1010 multiplier/accumulator. This team sends power and performance on their separate ways. One up . . . the other down.

The innovative 74AS888 has an instruction-to-Y output of 46 ns maximum, or a 51% improvement over the 4-bit competition. Power dissipation is only 1.5 W maximum during operation.

Multiplies and divides are about as fast as additions. Flexible micro-instructions let you tailor an application-precise instruction set. You can use any software. Any word length in 8-bit increments. Emulate any known µP instruction set while achieving improvements in execution speeds.

™ Trademark of Texas Instruments Incorporated

The 74AS888 is fully supported and readily available through TI distributors so you can get your system design finalized in minimum time.

TI's new THCT1010 is pin-for-pin compatible with the industry-standard multiplier (TDC1010J) but consumes 30 times less power. In conjunction with the 74AS888, it can significantly cut the power requirements of bit-slice systems.

Fabricated in silicon-gate CMOS, the THCT1010 is a 16- × 16-bit multiplier with 35-bit accumulator. How fast is it? For the -100 suffix, 100 ns maximum with a worst-case power consumption of only 150 mW.

If you want more details on the 74AS888 and THCT1010, just dial the 800 number below or clip and mail the coupon.

For quick response to your information needs, call Texas Instruments today at **1-800-232-3200.**

27-5287

Texas Instruments Incorporated
P.O. Box 809066
Dallas, Texas 75380-9066

Expires June 30, 1986
SPR103ED500C

YES, please send me the information checked below.

- PR22 ☐ TMS32020 Applications Handbook
- PR25 ☐ TMS32020 User's Guide
- PR12 ☐ TMS32020 Third-party Support
- PR30 ☐ Digital Signal Processing Newsletter
- DB01 ☐ IMPACT 74AS888 8-bit-slice Processor Data Sheet and User's Guide
- CL04 ☐ THCT1010 CMOS Multiplier/Accumulator Data Sheet

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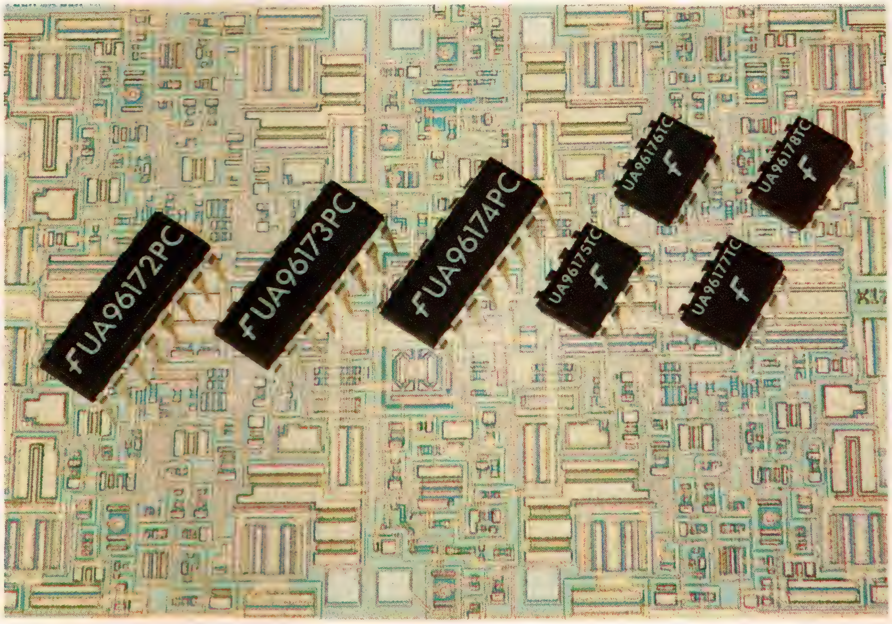
Serial datacomm driver/receiver ICs furnish higher data rates, lower power consumption

Denny Cormier, *Western Editor*

Line drivers and receivers for RS-232C lines are falling in cost, and many are now being fabricated in CMOS to meet demands for higher performance and lower power consumption in standard, single-ended, serial data terminal equipment (DTE). More demanding applications—calling for serial transmission rates in the megabaud range over long multipoint party lines—are inspiring a new generation of line drivers and line receivers. These ICs can handle not only the RS-422A-standard differential (balanced) line but also RS-485 party-line standards.

Your datacomm-network design initially determines the standard you'll employ, but choice of a standard needn't complicate upgrades of and changes to the network. RS-232C designs can be upgraded to RS-423A unbalanced-line standards (see **Ref 1**). By converting your unbalanced-line interface to the RS-422A standard, you can achieve higher noise rejection at data-transmission rates as great as 10M bps over a 40-ft length of twisted-pair cable. Indeed, many new line drivers and receivers support more than one standard.



***You can design an entire RS-485 multipoint party-line system** with the μA9617X Series differential line-driver, -receiver, and transceiver ICs from Fairchild Semiconductor. This chip set is also compatible with the RS-422A and RS-423A interface standards.*

RS-232C still viable

Don't think, however, that the RS-232C standard has been outdated. The simplicity and economy of the Electronic Industries Association's RS-232C interface have made it the most widely used interface for general-purpose, point-to-point serial datacomm networks that communicate at speeds below 20k bps over maximum cable lengths of 50 ft. In fact, the military has adopted the RS-232C standard as MIL-STD-188C/100. The standard is also supported by the European CCITT V.24 and V.28 recommendations and by the International Standards Organization's 2110 specifications. With the impetus from the CCITT's Integrated Services Digital Network (ISDN), which will incorporate the RS-232C interface, the popularity of the RS-232C interface has continued to gain momentum.

If you are planning to employ a low-cost, RS-232C serial interface, consider National Semiconductor's DS1488/89 line-driver/receiver ICs. The price of the DS1488/89 is $0.30 (1000). Exar Corp, Fairchild Semiconductor, Motorola, Signetics, and Texas Instruments are alternate sources for the chips, and these companies offer other TTL-compatible driver/receiver ICs having similar specs.

No matter which line receiver you choose, you'll have to take steps to control your line driver's wave shaping to remain within the RS-232C spec. Wave shaping becomes particularly important when you're using line receivers—like those from Motorola and Texas Instruments—that use hysteresis to reduce noise. Dale Pippenger, manager of applications engineering for TI's linear division, recommends that you use trimming capacitors on the outputs of your line drivers to keep rise times at 4% of the nominal signal duration. For example, a 15-ft length of standard twisted-pair cable with a typical capacitance of 52.5 pF/m would yield a total cable capacitance of about 230 pF. To stay within a slew rate of 20V/μsec, the line driver's output capacitance should be approximately 500 pF. Therefore, you should configure each output of a standard RS-232C

Kyocera high speed clock oscillators have shattered the CMOS time barrier.

Kyocera announces a revolutionary breakthrough in clock oscillators for CMOS-based computers, peripherals and telecommunications applications. Now our clock oscillator family offers the dual advantages of the highest CMOS clock speeds and driving capability on the market and low power consumption as well.

World's fastest clocks for CMOS and TTL logic.

To meet the needs of today's and tomorrow's high speed gate arrays, Kyocera's KXO-HC clock oscillator spans a frequency range of 500 kHz to 50 MHz and can drive up to 100 pF loads, up to 10 TTL gates. Yet it consumes only 16mA at 24 MHz. This low power reduces heat in the circuit, which increases reliability. And, reduces power supply costs in the process.

Tri-state for easy circuit testing.

In addition, our KXO-HC & TS models offer our tri-state capability which allows them to disable during testing and decouple from the oscillator bus when a control signal is applied. This lets circuit designers test the entire circuit board with an external synchronizing signal. Plus, it allows the circuit to be tested utilizing less expensive, lower power test equipment.

Pin 7 case ground for improved shielding.

The Kyocera KXO family of clock oscillators are hermetically sealed to protect them from humidity. And, are designed with the number 7 pin grounded to the case and an all-metal package which helps minimize RF radiation and meets FCC EMI specifications.

KXO Series	Frequency Range	Fan Out	Drive Level	Features
KXO-HC	500 kHz - 50.0 MHz	10 TTL	CMOS	HCMOS, TTL, Tri-state (Disable & Decouple)
KXO-01	4.0 MHz - 50.0 MHz	10 TTL	TTL	Economical Cost
KXO-TS	8.0 MHz - 34.0 MHz	10 TTL	TTL	Tri-state (Disable & Decouple)
KXO-CL	50.0 Hz - 8.0 MHz	1 LSTTL	CMOS	CMOS, Low Power
KXO-CS	250 kHz - 24.0 MHz	1 TTL	CMOS	HCMOS, Low Power, Stand by function

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CIRCLE NO 54

line-driver IC (such as TI's SN75188) with a 270-pF capacitor to ground **(Fig 1).**

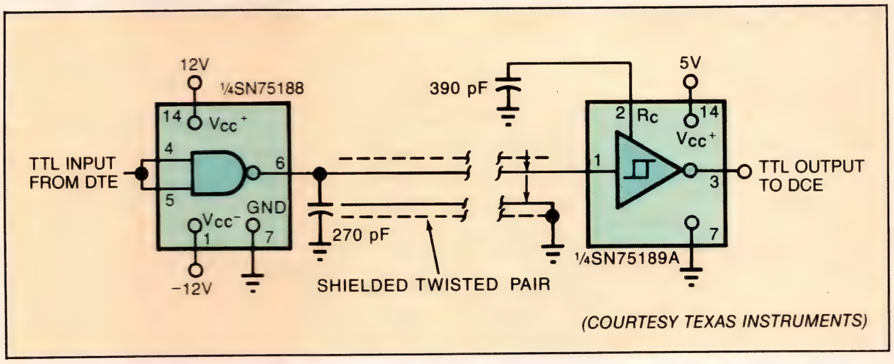


***Fig 1—To remain within the 30V/µsec rise time** defined by RS-232C standards, you must trim line-driver outputs with an external capacitor to compensate for differences in cable capacitance.*

You might want to consider RS-232C line-driver/receiver ICs for applications other than datacomm interface links. **Fig 2a** shows an example of a logic-level translator for DTL-to-RTL or DTL-to-MOS conversion. The circuit uses a Motorola MC1488 quad line-driver chip. **Fig 2b** shows a design for an MOS-to-TTL level translator using Motorola's MC1489 line receiver. These circuits, which come in 14-pin DIPs, help cut component count, particularly when you can take advantage of spare stages in the quad driver/receiver ICs.

You can achieve even denser component packing with the NE5170 octal line driver and NE5180/81 octal line receivers from Signetics. These parts sell for $4.50 (100) and come in 28-pin DIPs or surface-mount plastic leaded chip carriers (PLCCs).

Manage heat dissipation

When heat dissipation or battery operation is a major concern, as is the case with miniaturized or battery-driven devices, you should consider a low-power RS-232C driver/receiver IC like the Max232 dual transceiver from Maxim Integrated Products. Fabricated in CMOS, the Max232 only uses 5 mA of quiescent current from a single 5V supply, yet its internal charge-pump circuitry generates ±10V to switch RS-232C signal levels. The part's line-receiver pair uses 0.5V of hysteresis to improve noise reduction. Available in either a 16-pin surface-mount package or a plastic DIP, the commercial-grade (0 to 70°C) Max232 sells for $3.60 (100).

National Semiconductor plans to introduce its CMOS DS14C88/89 line-driver/receiver parts this quarter. According to preliminary data from National, the DS14C88 line driver will dissipate only 200 µA of static power-supply current, which represents a 99% reduction in power consumption compared with the company's DS1488/89 bipolar counterparts. The CMOS driver/receiver chips will each cost $0.60 (1000). TI intends to follow suit early this year with the introduction of its low-power quad SN75C188/89 driver/receiver ICs. The company manufactures these devices using combined bipolar-CMOS (BiMOS) technology.

Watch for common-mode noise

Common-mode noise rejection remains the most significant problem you will face when designing an

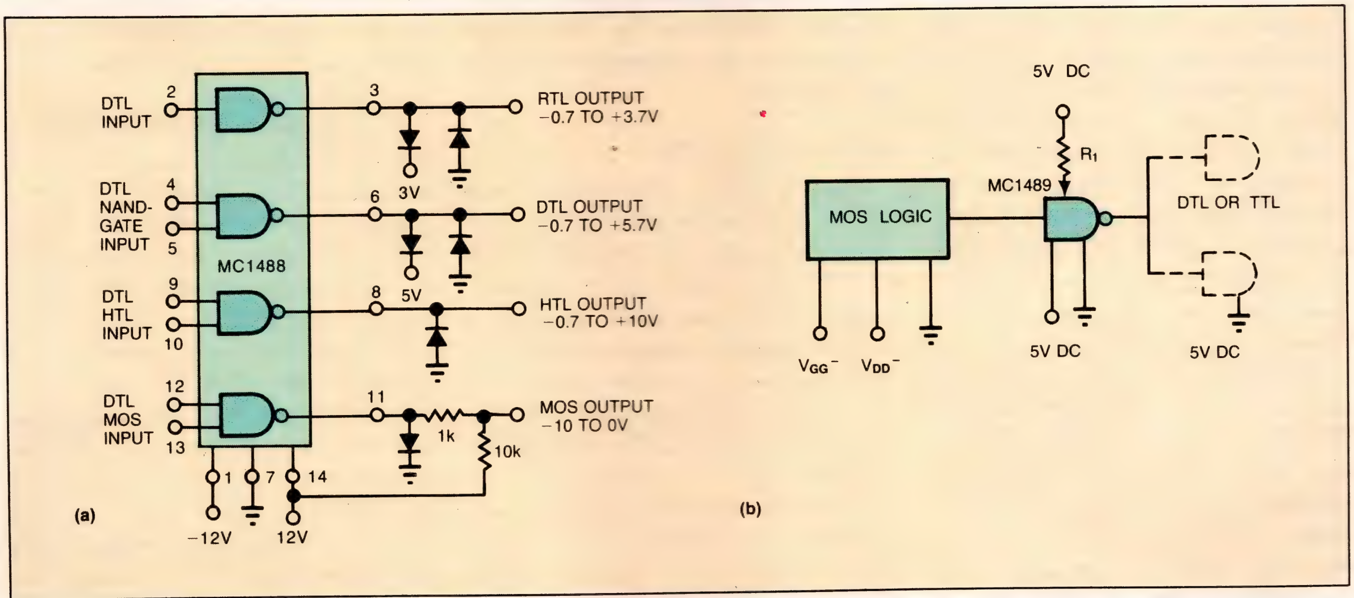
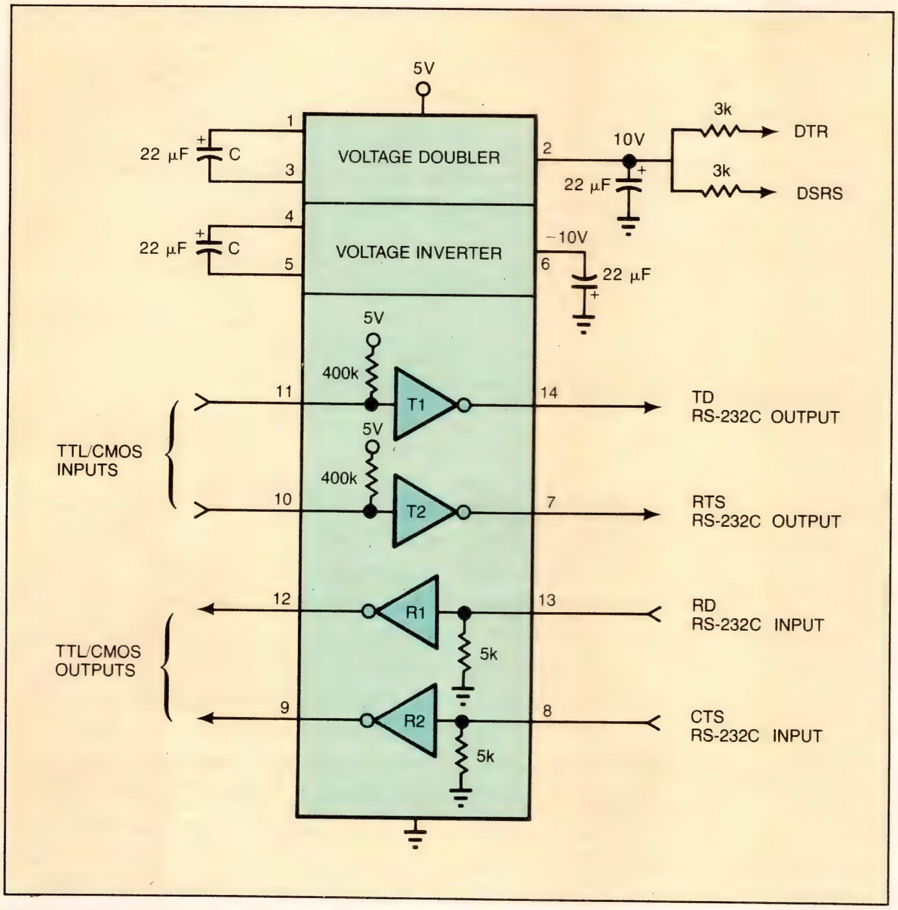


***Fig 2—In addition to functioning as a single-ended EIA interface component,** an unbalanced MC1488 line driver from Motorola can serve as a level translator to link bipolar TTL circuits with RTL or CMOS logic **(a)**. In addition, an MC1489 line receiver can double as a level translator to connect CMOS with DTL or TTL logic **(b)**.*



For low-power operation from a single 5V supply, *the CMOS Max232 transceiver from Maxim Integrated Products provides a dual RS-232C bidirectional interface. An on-chip charge pump internally converts the single 5V supply voltage into ±10V.*

interface between the DTE and the data circuit-terminating equipment (DCE—modems and the like). In general, common-mode noise arises from differences in ground-level potentials between DTE and DCE. If you're finding too much common-mode noise on your single-port connections, or if you need more than 50 ft of cable between your computer and peripherals, you may want to try upgrading your RS-232C interface into one that uses RS-423A line-driver/receiver ICs.

The EIA developed the RS-423A and the now virtually obsolete RS-449 electrical specifications to deal with 100k- and 2M-bps transmission rates, respectively, over unbalanced lines. In addition to meeting the CCITT V.10 and X.26 recommendations, RS-423A specifications comply with US Federal Information Processing Standard 1030A. Because of crosstalk and common-mode noise, designers generally prefer balanced interfaces to RS-449 interfaces for high-speed communications between computer peripherals.

Multistandard ICs

To deal with a wide range of today's data-transmission applications, and with the increased common-mode noise accompanying higher data transmission rates, you should consider using multistandard driver/receiver ICs in your serial datacomm interfaces. For example, a design using AMD's Am26LS30 differential line-driver and Am26LS32 line-receiver chips can operate with either RS-232C or RS-423A interfaces by grounding the inverting terminals. You can achieve similar results with other RS-422A driver/receiver ICs, such as Motorola's MC3487/86 and TI's SN75172/73. In RS-422A operation, these parts will yield serial-interface designs for systems that communicate at rates to 10M bps.

Another multistandard part, Linear Technology's quad LT1032 RS-232C line driver, incorporates low-power Schottky circuitry and draws a maximum steady-state current of 1.0 mA from a ±15V dual supply. The device is pin compatible with DS1488 parts in 14-pin DIPs. Its drive capacity is sufficient to handle the greater fanout (10 receivers per driver) and data rate of the RS-423A interface, and it can also handle the conversion, without a transformer, of ±5V into ±15V. The latter capability saves board space and cuts op-amp power-supply costs. The LT1032 sells for $2.95 (100).

Even the RS-422A standard, however, cannot adequately deal with party-line contention, and it still lacks sufficient common-mode noise rejection for multipoint connections. The inability to resolve bus contention can lead to forced overloads, excess heat dissipation, and, as a consequence, damage to the output stages of your line drivers. To prevent permanant damage, most differential line-drivers simply go into a thermal-shutdown mode during a contention-induced overload situation.

In response to the noise-rejection and contention problems, the EIA introduced the RS-485 party-line standard in 1983. Without losing either the wide bandwidth or the excellent common-mode noise rejection of the RS-422A balanced line (the maximum common-mode voltage of the RS-422A standard is 6V, −0.25V), the RS-485 party-line standard lets you connect 32 line drivers, receivers, and transceivers (ie, driver/receiver pairs) in the same network. The standard calls for transceivers with 3-state outputs to resolve bus contention.

Manufacturers have introduced several chip sets that handle the

RS-485 party-line interface. You can add single interface stations to your RS-485 party line with National's 3-state DS3695/96 differential transceivers and DS3697/98 differential-repeater ICs. These ICs come in 8-pin miniature DIPs. In plastic DIPs, the -95 and -97 parts cost $1.75, and the -96 and -98 parts cost $1.85 (100). Texas Instruments is a second source for these parts with its SN75176 transceiver and SN75178 repeater chips.

If you already have a system using RS-422A balanced interfaces, you may upgrade it to RS-485 standards by retrofitting with TI's SN75172/74 3-state line drivers and SN75173/75 line receivers. According to the company, these parts are plug-in replacements for conventional RS-422A driver/receiver ICs, including the Am26LS31/32A and the MC3487/86. The TI parts cost $1.78 (1000) in plastic DIPs.

Last year, Fairchild Semiconductor introduced its µA96176 differential bus transceiver and µA96177/78 differential bus repeaters, specifically for use with RS-422A or RS-485 interface standards. The transceiver and the repeaters sell for $0.90 (100). According to Steve Kaufman, marketing manager for Fairchild's interface products division, you can assemble multistandard RS-423A, -422A, or -485 serial interfaces on high-density boards by pairing the company's µA96172/74 quad differential line drivers with its µA96173/75 quad line receivers, which come in both ceramic and plastic 16-pin DIPs. The cost is $1.45 for the line drivers and $1.25 (100) for the receivers.

EDN

Standards documents

The Electronic Industries Association publishes its recommended standards along with details concerning electrical specifications and serial datacomm interface applications. You may purchase documents relating to these topics by writing to:
Electronic Industries Association
Engineering Department
2001 Eye St NW
Washington, DC 20006.

Reference

1. Pippenger, Dale, "ICs extend RS-422 to multistation applications," *EDN*, March 21, 1985, pg 181.

Article Interest Quotient
(Circle One)
High 506 Medium 507 Low 508

For more information . . .

For more information on the serial driver/receiver ICs described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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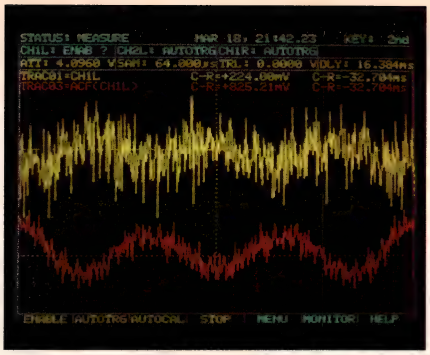

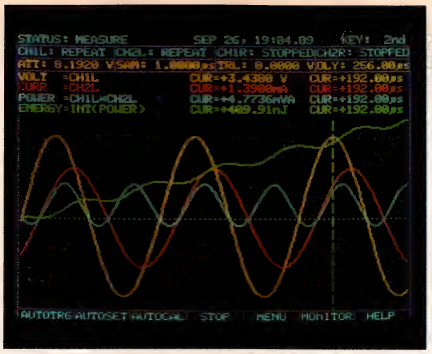

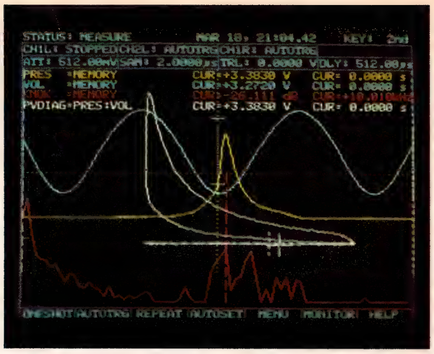

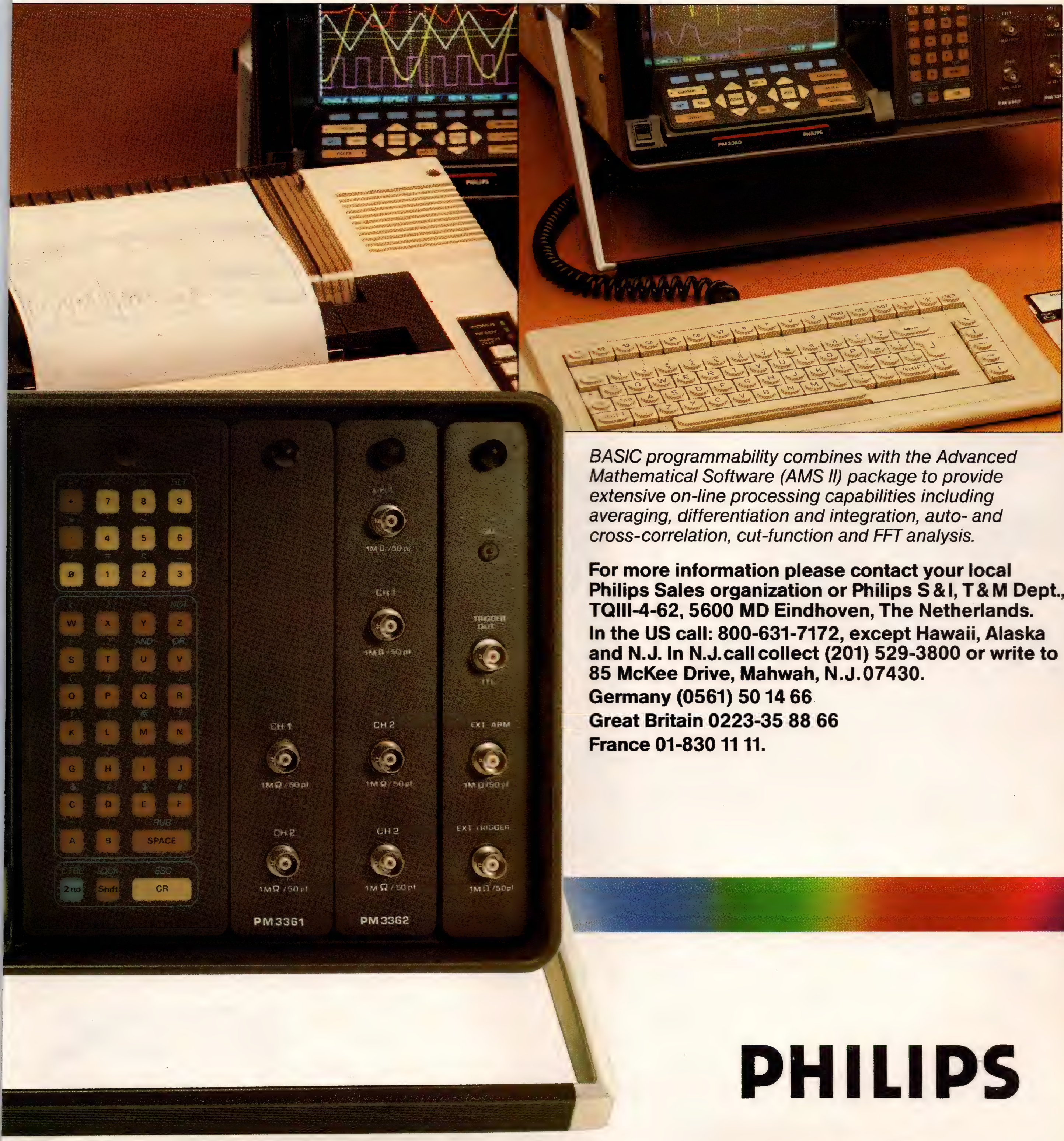

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CIRCLE NO 57

Switched-capacitor lowpass-filter IC eliminates dc offset, low-frequency noise

Because its architecture places it outside a system's dc signal path, the LTC1062 switched-capacitor lowpass filter **(Fig 1a)** makes no contribution to the system's dc offset voltage and low-frequency noise. The monolithic device is a fifth-order, all-pole, maximally flat filter. The filter uses an internal clock whose frequency you can set by connecting an external capacitor; you can also use an external clock whose frequency is as high as 4 MHz.

Fig 1b shows a typical configuration of the LTC1062 as a lowpass filter. In this configuration, an external 100-kHz clock drives the fil-

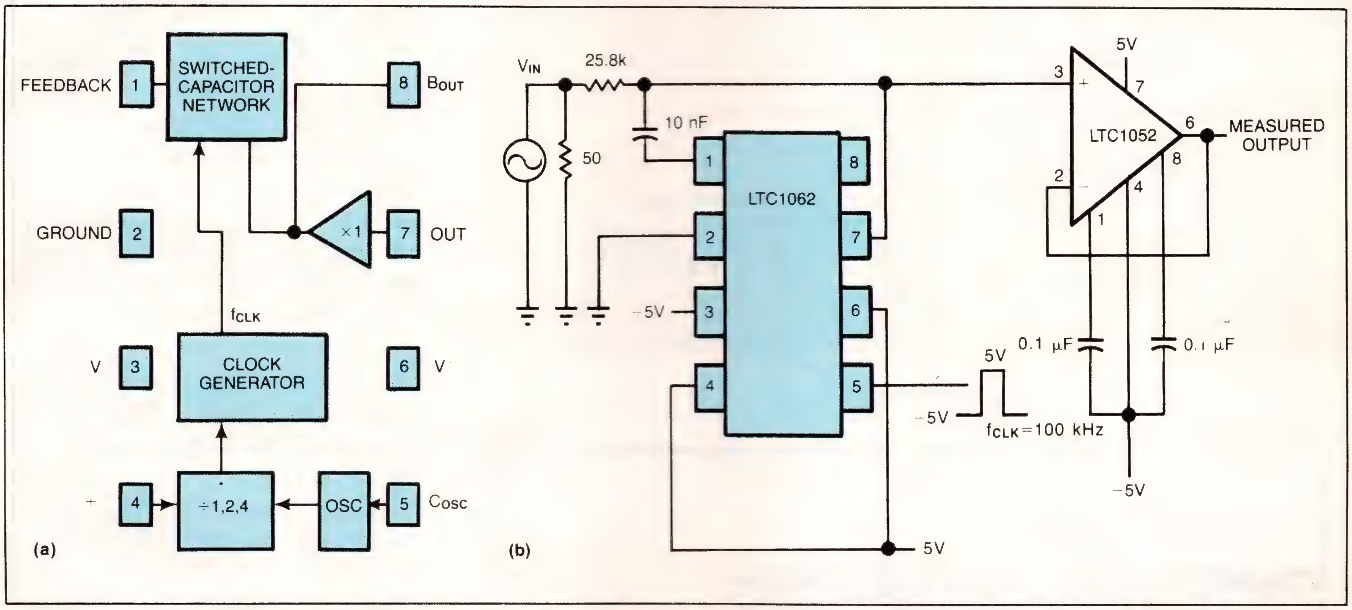


*Fig 1—**Silicon-gate CMOS is the process of choice** in the LTC1062 switched-capacitor, fifth-order lowpass-filter IC **(a)**. In the test circuit **(b)**, the device uses a 100-kHz external clock to provide a 1-kHz cutoff frequency.*

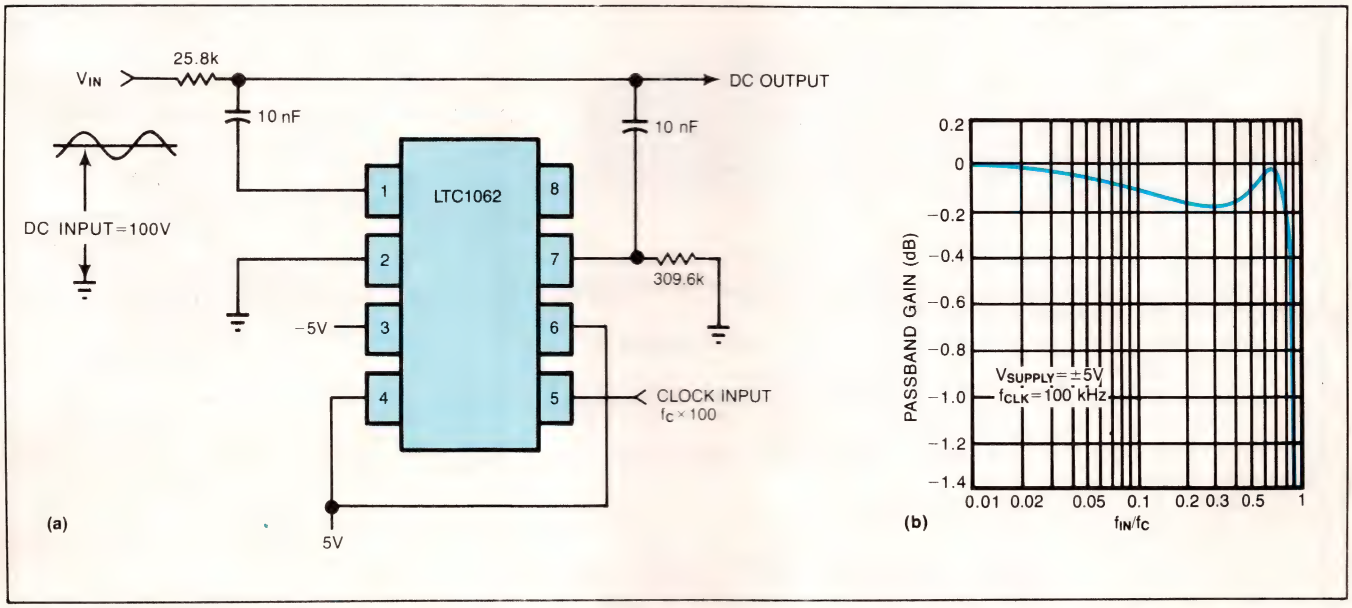


*Fig 2—**Lacking any dc connection to the dc signal line,** this circuit **(a)** removes ac signals greater than 1 kHz from the dc line. The curve in **b** shows the sharp cutoff characteristic and the low (<0.2-dB) ripple.*

ter. The clock-to-cutoff frequency ratio is 100:1. Measurements show that frequency response is typically 0.02 dB down at half the cutoff frequency and 30 and 60 dB down at twice and four times the cutoff value, respectively.

The filter works by sampling its own input and output across an external resistor. An external capacitor couples the IC to the signal. The external RC pair reacts with the device's internal switched-capacitor network to provide a fifth-order rolloff at the output. You can connect two LTC1062s in cascade to obtain a tenth-order lowpass filter.

A typical application for the LTC1062 is a circuit that filters ac signals from high dc voltages (**Fig 2a**). In the configuration shown, the IC uses a 100-kHz clock frequency and provides a 1-kHz cutoff frequency. The filter accurately passes the signal's dc level and acts as a fifth-order lowpass filter for ac signals riding on the dc signal. **Fig 2b** gives the passband amplitude response of **Fig 2a**'s circuit.

Useful for input frequencies from 0 to 20 kHz, the LTC1062 operates from single or dual power supplies whose total voltage span can range from 5 to 18V. The filter comes in two versions, which cover operating-temperature ranges of −40 to +85°C and −55 to +125°C. Packaged in an 8-pin plastic or hermetic DIP, the filter IC draws 7 mA max at 25°C and 10 mA max over temperature. LTC1062CN8, $3.55; LTC1062MJ8, $7 (100).

—Bill Travis

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 942-0810.

Circle No 730

Monolithic quad matched-transistor array specs ≤2% beta matching for all devices

A quad monolithic npn-transistor array, the MAT-04, offers close matching of transistor parameters. The manufacturer tests all possible pairs of the quad for offset voltage ($V_{BE1}-V_{BE2}$), input offset current ($I_{B1}-I_{B2}$), and gain (h_{FE}) match. The array is available for operation over two temperature ranges: Units with -E and -F suffixes are specified over −25 to +85°C; models with -A and -B suffixes perform over −55 to +125°C.

At 25°C, the highest-grade models (MAT-04A and -04E) spec 400 min, 800 typ h_{FE}. The reduced-spec models (MAT-04B and -04F) spec 300 min, 600 typ for this parameter. Gain matching is within 2% and 4% max for the high-grade and reduced-spec units, respectively. Respective offset voltages for the two units are 150 and 300 μV max, and maximum input offset currents (at I_C=100 μA) are 5 and 13 nA.

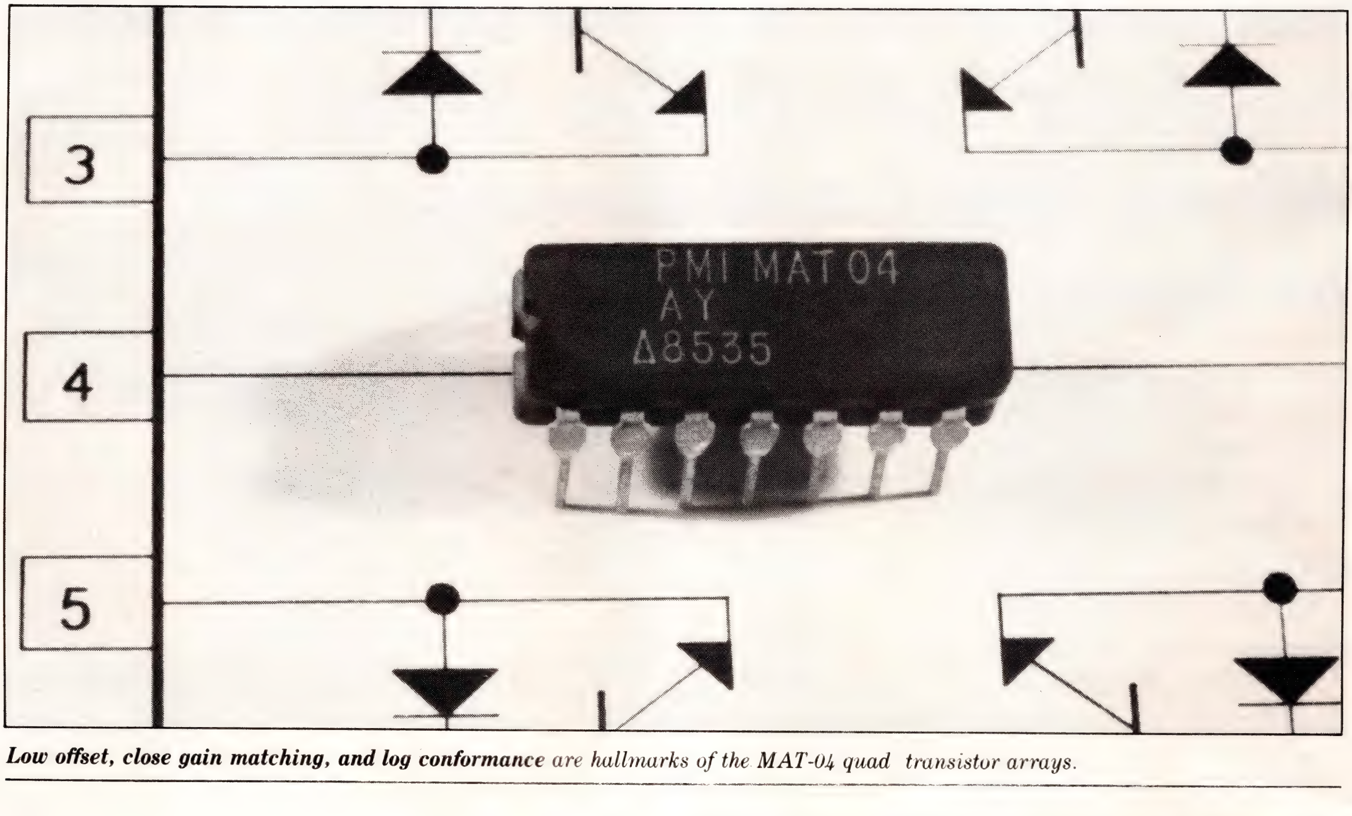
Over −25 to +85°C, the high-grade MAT-04E specs an h_{FE} of 225 min, 625 typ. Maximum offset voltage is 210 μV. Corresponding specs for the reduced-spec Model MAT-04F are an h_{FE} of 200 min, 500 typ and a maximum offset voltage of 420 μV. Over −55 to +125°C, the high-grade MAT-04A specs h_{FE} of 175 min, 475 typ and the reduced-spec -04B specs 125 h_{FE} min, 425 h_{FE} typ. Respective maximum offset voltages for these two models are 250 and 500 μV max.

At 25°C, all units spec 40V min BV_{CEO}, 60-mV max $V_{CE(SAT)}$ (at I_C=1 mA), 5-pA typ I_{CBO}, and 300-MHz typ gain-bandwidth product. Noise specs for the MAT-04A/E and -04B/F are 3 and 4 nV/$\sqrt{Hz}$ max at V_{CB}=0V and f_0=10 Hz. Input and output capacitance for all units is 40 and 10 pF typ, respectively.

The MAT-04 quads incorporate protection diodes across each base-emitter junction. According to the manufacturer, these diodes ensure long-term stability of matching parameters by preventing parameter degradation that could otherwise arise because of reverse-bias base-emitter current. The manufacturer claims that the transistors offer very close logarithmic conformance; they're therefore suitable for use in log and antilog circuits. Packaged in 14-pin epoxy and hermetic DIPs, the industrial- and military-range devices cost $5.40 and $10.40 (100), respectively.—***Bill Travis***

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. TWX 910-338-0218.

Circle No 727



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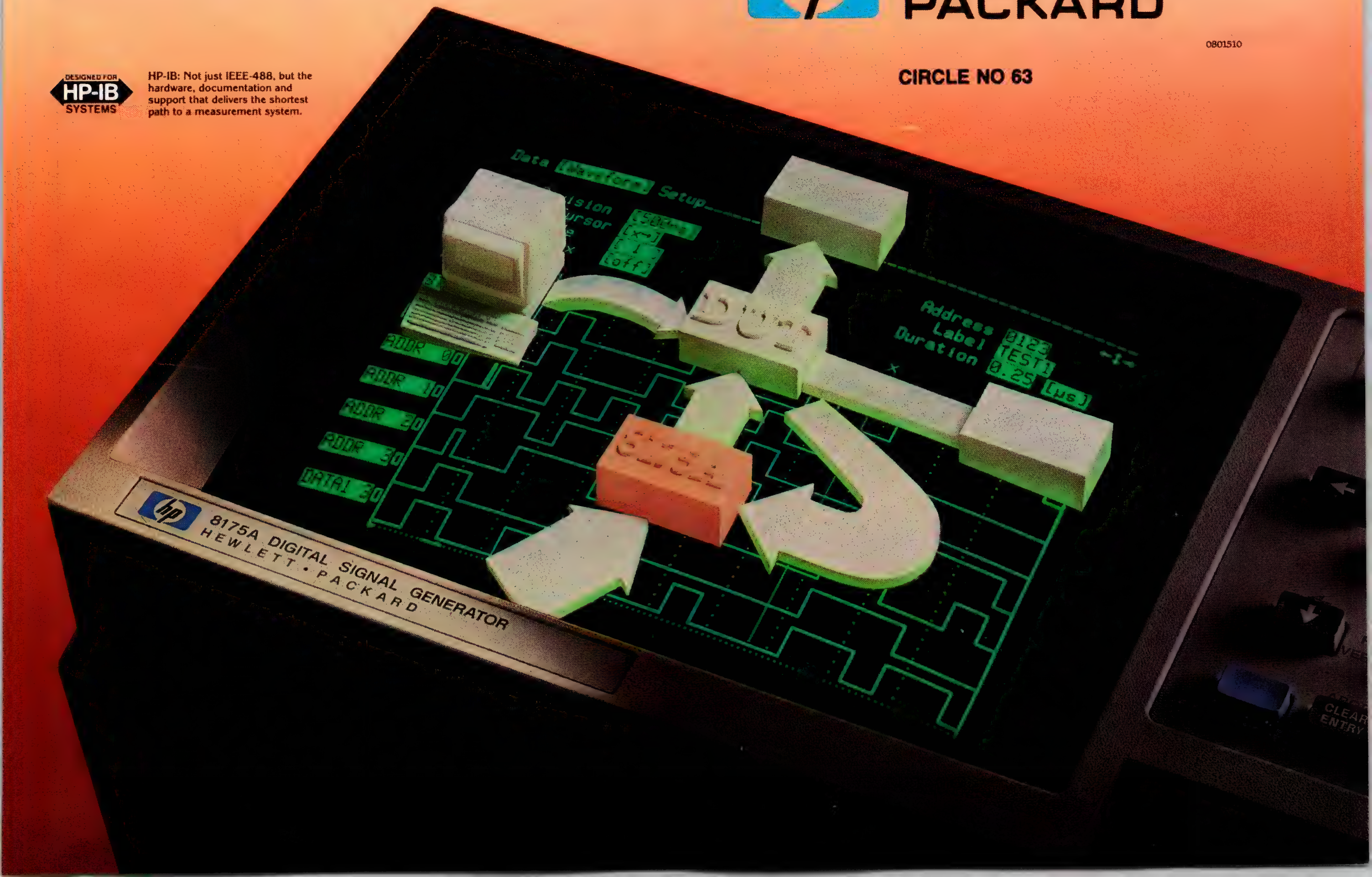


Successive-approximation A/D converter delivers 12-bit output in 1.56 μsec

The Model HAS-1202A 12-bit hybrid D/A converter, an enhanced version of the HAS-1202, converts in 1.56 μsec max, vs its predecessor's 2.86 μsec. In both converters, a high-speed, current-output D/A converter works in conjunction with a comparator and a successive-approximation register. The devices also contain timing circuitry, as well as a voltage-reference block that imparts a 10.24V full-scale analog-input range to the converters.

If the 10.24V input range seems unusual (most converters use a multiple of 5V), note that this range yields a least significant bit (LSB) of exactly 2.5 mV, vs the 2.44 mV that's inherent in a 10V-range converter. By connecting the appropriate pins, you can configure the device's input for either 0 to 10.24V unipolar or ±5.12V bipolar input ranges. Output coding is straight binary; that is, the most negative input voltage in the input range produces all zeros and the most positive yields all ones.

Capable of operating at conversion rates as high as 641 kHz, the HAS-1202A is able to digitize input signals possessing frequency components as high as 320 kHz. Note that to obtain this digitizing rate, you must use a track/hold amplifier to ensure that the converter's input voltage does not change by more than ½ LSB during the 1.56-μsec conversion period. (The manufacturer's HTC-0300A track/hold amplifier is suitable for this purpose, as is the industry-standard 4860 type.)

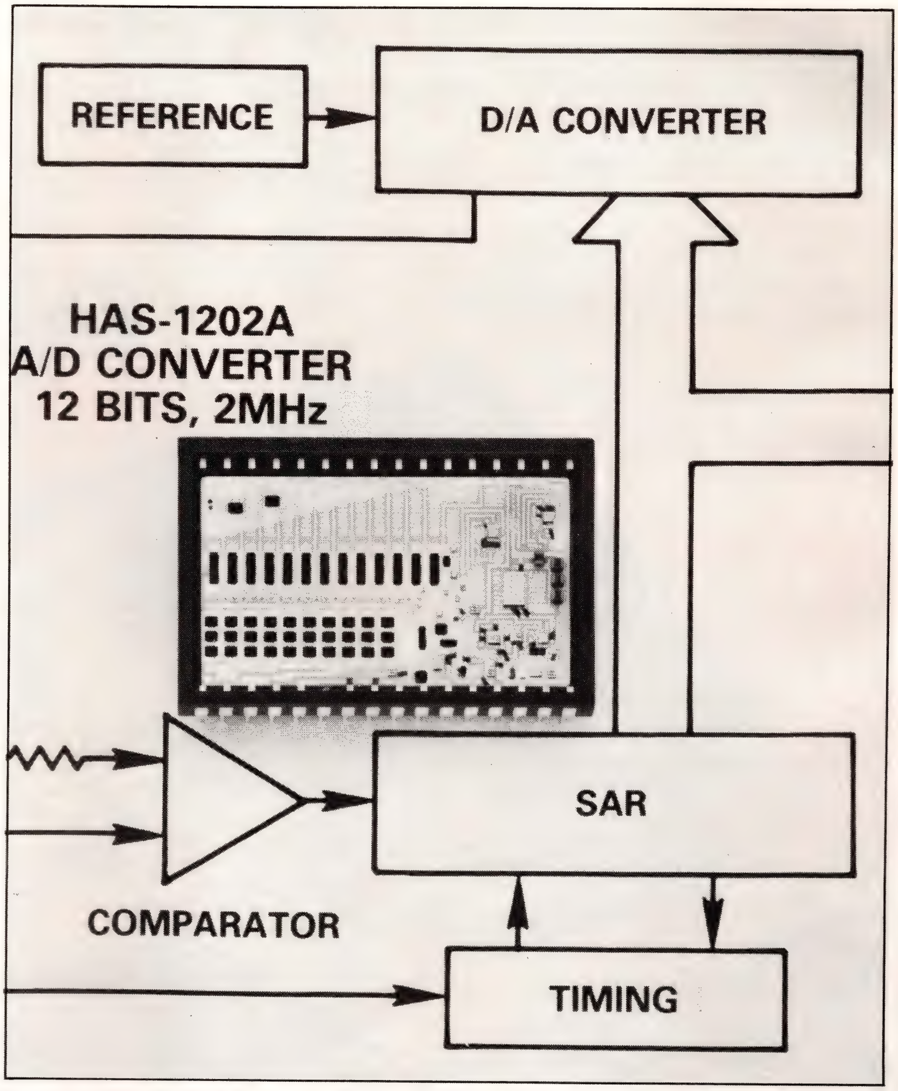
The 1202A offers guaranteed monotonicity at 25°C. The use of the term "monotonicity," however, is a misnomer—*all* successive-approximation A/D converters are monotonic (ie, output codes never decrease as input voltages increase). The manufacturer confirms that the data sheet should instead read "no missing codes" at 25°C. Typical integral and differential nonlinearity at 25°C is ±½ LSB, and linearity drift is 3.5 ppm/°C typ.

Available for operation over three temperature ranges (0 to 70°C, −25 to +85°C, and −55 to +100°C), the HAS-1202A comes in a 32-pin, triple-wide ceramic or metal DIP. Units that operate over −55 to +100°C receive screening to MIL-STD-883. Operating from ±15 and 5V supplies, the converter dissipates 1.9W max. From $175 (100).

—Bill Travis

Analog Devices Literature Ctr, 70 Shawmut Rd, Canton, MA 02021. Phone (919) 668-9511.

Circle No 728



Nearly twice as fast as the earlier HAS-1202, *the HAS-1202A 12-bit A/D converter converts in 1.56 μsec. The part, which is pin compatible with the earlier model, is also compatible with TTL logic levels. It delivers data in a 12-bit parallel format and accepts analog input voltages of ±5.12V or 0 to 10.24V.*

One-chip unity-gain difference amplifier specs 86-db CMRR and 0.01% gain error

Although the INA105 monolithic difference amplifier is deceivingly simple—an operational amplifier and four resistors—the chip provides specs that would be difficult to realize in a discrete circuit that you could build by yourself. For example, the amplifier's guaranteed worst-case common-mode rejection and gain error are 86 dB and 0.01%, respectively.

The specified nonlinearity (a spec that's often more important than the absolute-gain-error spec) of the INA105 is 0.001% max. A typical application that demands such a linearity spec is a 16-bit A/D-conversion system. One LSB at 16-bit resolution is 0.0015% of full-scale range. Therefore, the difference amplifier contributes ⅔ LSB max integral nonlinearity to the system. Note that the INA105's data sheet uses the best-fit straight-line definition for its nonlinearity spec—its end-point nonlinearity could, therefore, be as much as twice the specified value.

Operating from ±15V supplies, the amplifier delivers ±10V min output swing at currents as high as 20 and −5 mA. The 20-mA capability makes the device useful in 4- to 20-mA current-transmission systems. When the output is short-circuited to ground, current-limiting levels are 40 and −10 mA. Output impedance is typically 10 mΩ. The amplifier remains stable when driving capacitive loads as high as 1000 pF.

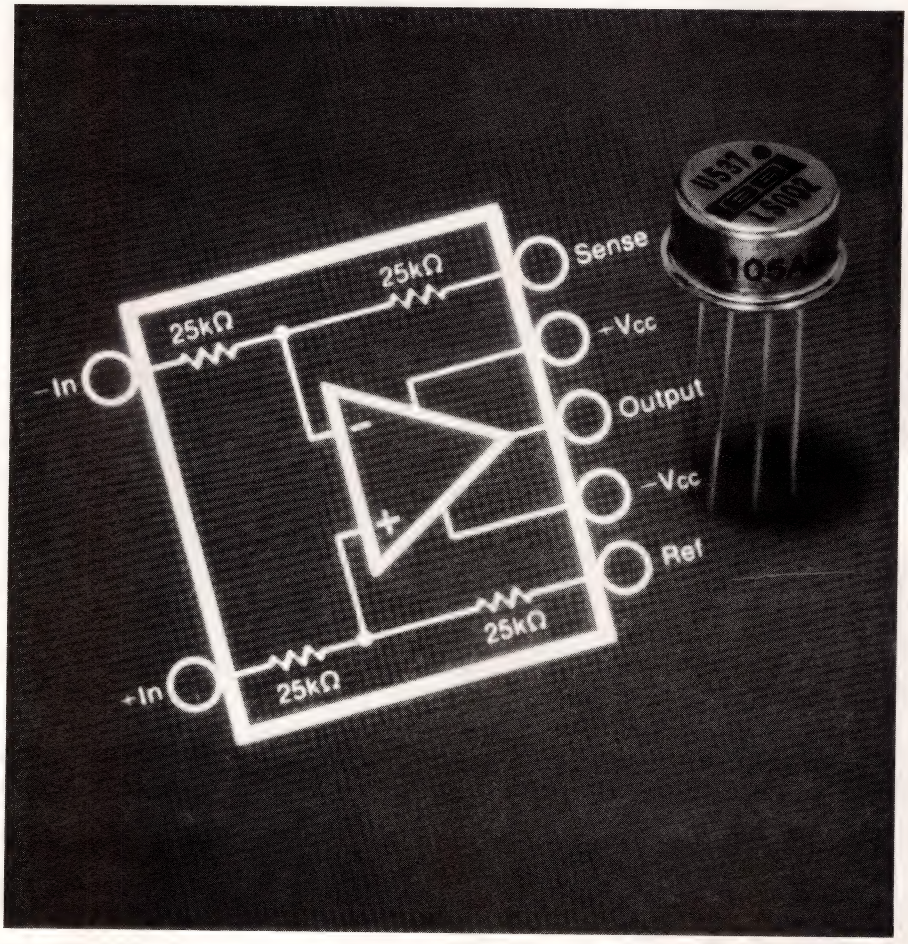
Differential and common-mode input impedance is typically 50 kΩ, and the inputs accept differential and common-mode input signals as high as ±10 and ±20V, respectively. Common-mode rejection over the −25 to +85°C operating range is 80 dB min for the INA105AM and 86 dB min for the premium-grade INA105BM. Initial offset voltage is 250 μV max for both grades, and offset drift is 20 and 10 μV/°C max for the -AM and -BM models, respectively.

Typical noise specs, which include the effects of the amplifier's input-current noise and the thermal-noise contribution of the resistor network, are 1.2 μV p-p from 0.01 to 10 Hz and 60 nV/$\sqrt{\text{Hz}}$ at 10 kHz. Small-signal and full-power bandwidths are typically 1 MHz and 50 kHz, respectively. The device's output slews at 2V/μsec min and settles a 10V output step to within a ±0.01% error band in 5 μsec typ.

Housed in a TO-99 (similar to TO-5) metal can, the INA105 draws ±2-mA max quiescent current. The unit operates from supplies ranging from ±5 to ±18V. Note, however, that all guaranteed specs are valid only for operation from ±15V supplies. Prices for the INA105AM and -BM are $5.75 and $7.20 (100), respectively.—***Bill Travis***

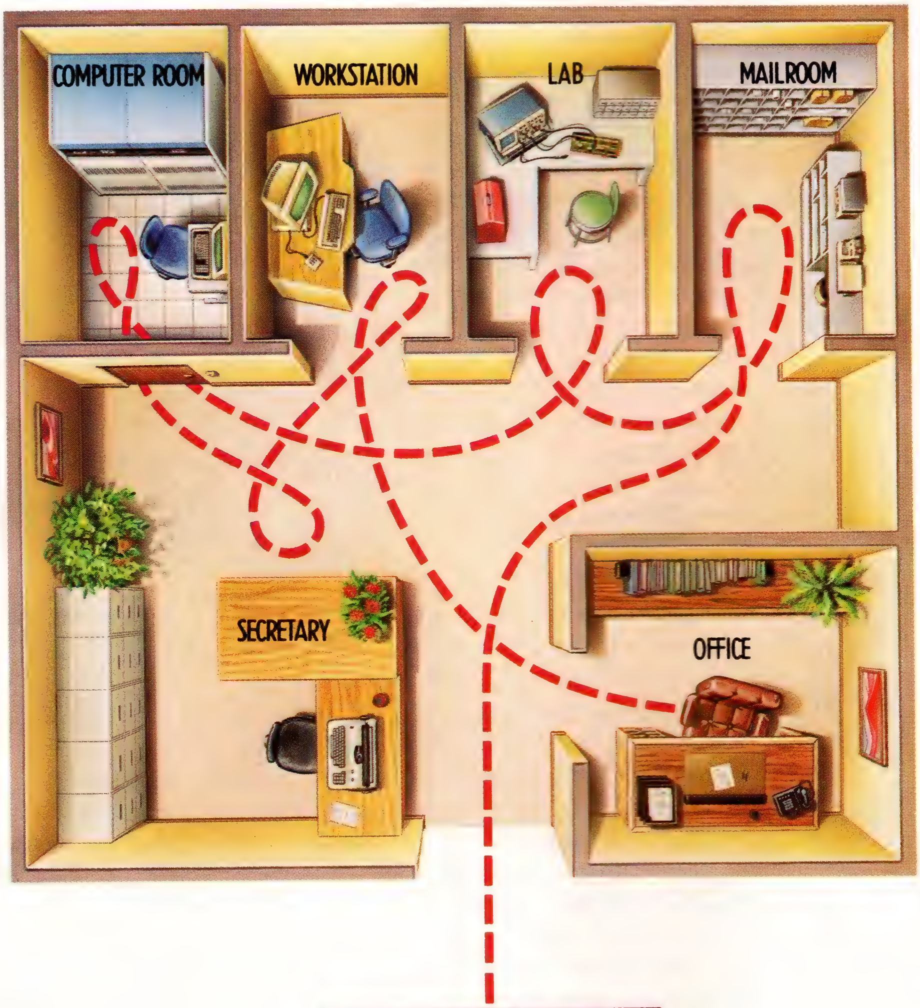
Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

Circle No 729



Simple topology and extremely tight specs *characterize the INA105 monolithic difference amplifier. The IC uses an on-chip, thin-film resistor network and a premium-grade operational amplifier to achieve its common-mode, gain-accuracy, and linearity specs.*

FOLLOWING A DESIGN ENGINEER AROUND ON A TYPICAL DAY CAN LEAD TO ONLY ONE CONCLUSION.



On any given day, design engineers are apt to be out of their offices as often as they're in.

To do design work, they have to park themselves in front of a workstation somewhere. For their documentation needs, they have to hover over a secretary. And it's back and forth throughout the organization to dispatch copies of their schematics.

Not only is this extraordinarily inefficient. Thanks to Workview,™ it's also entirely unnecessary.

Eminently affordable, Workview is the first and only IBM PC-based software program that addresses the three fundamental aspects of the design engineer's job—design, documentation and communications. All *integrated* under one easy to use, multi-windowed user interface, it's The Total Workday System.™

Workview supports analog, semicustom chip and design with standard parts. Its design facilities include a schematics editor and an interactive simulator with waveform I/O editing. Its documentation facility allows you to merge graphics and text. Finally, through Ethernet, Workview's communications facility provides for instant communication, pc to pc and pc to host.

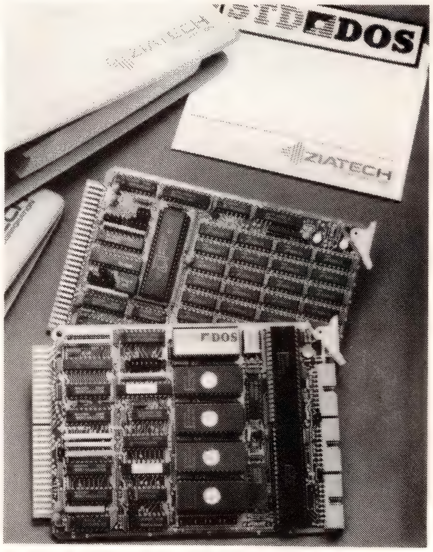
For more information, call us toll-free at 1-800-CAE-VIEW.
In MA, the number is 617-480-0881.

VIEWlogic™

CIRCLE NO 65

ROM-based OS makes STD systems MS-DOS compatible

Because it's fully compatible with PC-DOS, the STD DOS proprietary operating system for 16-bit STD Bus computers lets you use an IBM PC or compatible computer as a development system for industrial computer systems. An emulative operating system, STD DOS provides all the standard functions of MS-DOS in the appropriate format and furnishes an intelligent link between the target system and a PC. You can, therefore, take advantage of existing software modules and programs while developing new software for industrial applications.



In this target-system configuration, *a complete system resides on two STD Bus boards. STD DOS, an MS-DOS-compatible operating system, resides in ROM.*

Extending the file structure

For development applications, the operating system offers a few subtle improvements over MS-DOS. STD DOS supports four basic file types: PROM, RAM, disk, and remote. The PROM and RAM files are target-system files for storing the operating system, application programs, and data. The operating system can support a 320k-bit PROM and as much as 768k bytes of RAM.

Disk files can either be in the target system or in the development system. The target system can access a disk file in the development system—or in any IBM PC linked to the target processor via a serial port—by treating the disk file as a remote file. Labeling a file as remote allows the target system to access the file by name, so you don't need special communications software to access files.

The operating system comes with a DOS driver template and sample driver source code to help you write application-specific peripheral drivers for nonstandard I/O (like that of an automation system, for example). The BIOS and standard device-driver package provides easy access to most common system peripherals using PC DOS calls.

For software development on your PC, the vendor offers the DOS 8806-PCA (PC-assisted) system, which includes a 5-MHz 8088 CPU, a 320k-bit PROM, 256k bytes of RAM, a serial port, five counter/timers, a peripheral controller, two parallel ports, a card cage, and STD DOS development software and firmware. The package starts at $1995.

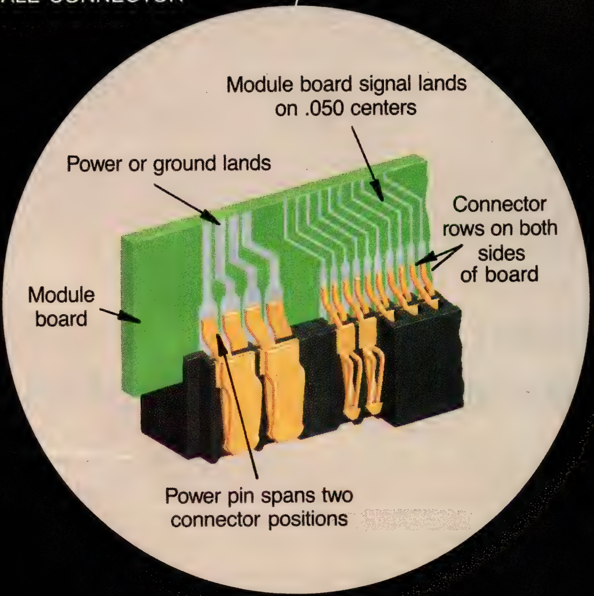
The vendor also offers the STD DOS firmware with a 2-board target system (DOS 8806-TS) that includes the firm's ZT 8806 CPU card and ZT 8823 RAM card. These cards also feature a 5-MHz 8088 CPU, a 192k-bit PROM, 256k bytes of RAM, a serial port, five counter/timers, a peripheral controller, and two parallel ports. DOS 8806-TS, from $995.—***Ed Teja***

Ziatech Corp, 3433 Roberto Ct, San Luis Obispo, CA 93401. Phone (805) 541-0488.

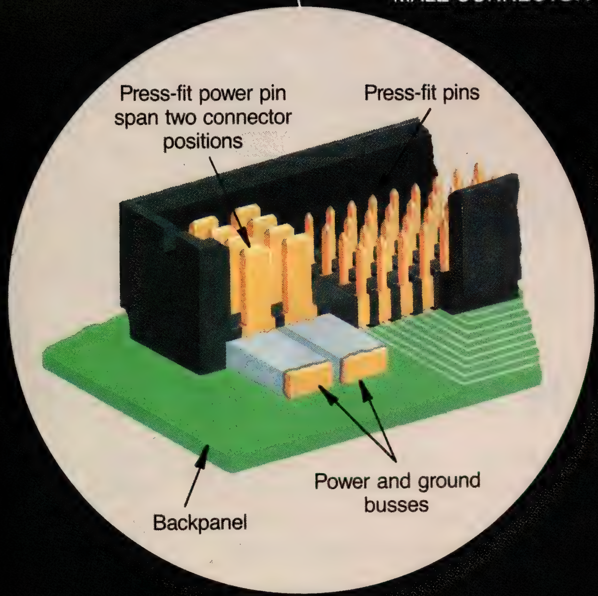
Circle No 731

Elfab Introduces: The Four Row Box Pac.™ High Density Interconnection at its best.

FEMALE CONNECTOR



MALE CONNECTOR



- High density interconnect system with 4 rows on .100″ grid.
- Shortest conductor path between module board and backpanel, with consistency of distance between all four rows
- Optional power and ground busses
- Optional Keying
- Low insertion force
- Male press-fit design or solder tail
- Early mate power pins
- Female surface mount adapts to either vapor phase or reflow soldering

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Elfab Corporation
1097 Yates
Lewisville, Texas 75067
214/221-8776
or call toll free:
1-800-527-0753

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(061)-27600 Telex: 70150

ELFAB
INTERCONNECTION INNOVATORS

CIRCLE NO 68

The Fastest Part About This Car Is the Workstation that Produced It—UltraGraf® III.

Lundy's new UltraGraf III is the fastest 3-D color workstation in its price range. And that means higher productivity in many applications.

Zero to 200,000 in One Second

But don't take our word for that. Take charge of the controls and put this incredible new machine through its paces. Feel the responsiveness of a double-buffered graphics engine that processes over 200,000 short vectors per second—in vivid color. Experience the breath-taking speed and precision of UltraGraf III as it handles complex curves with ease. Or shift into 3-D multiwindow mode and display several designs at once on the large 19-in. screen.

Great Systems Development Mileage

The modular UltraGraf III displays up to 256 simultaneous colors from a palette of up to 16.7 million. It boasts double-buffered, noninterlace display resolution of 1024 by 1024, and communicates with various I/O devices via serial and 16-bit parallel interfaces. It also operates with many host computers. As such, it's easy to integrate UltraGraf III into many design systems.

To facilitate your systems development even further, Lundy offers a CORE standard software subroutine package and a seasoned pit crew—one of the largest service and support networks in the industry.

No other workstation takes you from starting line to production line faster than UltraGraf III. Contact: Graphics Marketing, Lundy Electronics & Systems, Inc., One Robert Lane, Glen Head, N.Y., 11545. (516) 671-9000.

LUNDY®

CIRCLE NO 69

Stainless-steel keyboards withstand harsh environments

Impervious to most cleaning solvents, oil, water, acids, and alkalines, Series MT-8700 stainless-steel membrane keyboards are suitable for use in industrial controls, food processors, aircraft, medical instruments, petroleum equipment, and other applications that are subject to extreme environmental conditions, such as exposure to the elements. The keyboards offer four switch-contact configurations: spst-NO (Form A), spst-NC (Form B), spdt (Form C), and dpdt (Form 2C).

Unlike standard polycon membrane switches, stainless-steel switches are impervious to ultraviolet rays. The etched keyboard characters are scratch resistant; multicolored keys and a nonglare surface are optional.

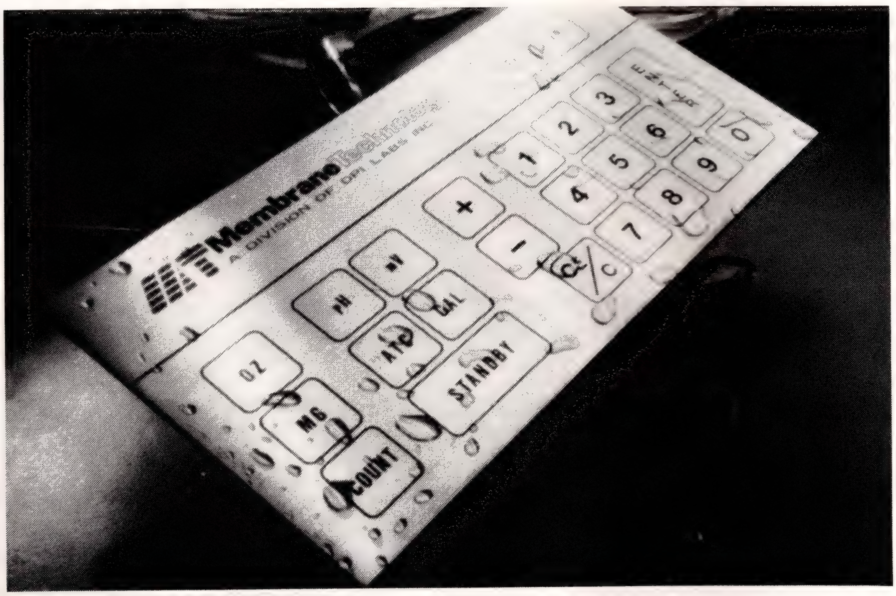
Electrical specifications for the keyboards include 0.1Ω contact resistance, and 10-MΩ insulation resistance at 100V dc. The switches' current rating is 200 mA at 6V dc. Nominal contact-bounce time for one of the switches is 1 msec. Dielectric strength between any two conductors measures 250V rms. For termination, the keyboards are available with connectors or pins. EMI/RFI shielding is optional.

Activating a key requires 6 to 12 oz of force; key travel distance is 0.015 in. The keyboards offer minimum lifetime specs of 3 million cycles per key and operate over −20 to +125°C. They can withstand 95% relative humidity at 50°C for 15 days.

Pricing for the keyboards depends on the switch type and number of stations you choose. In quantities of 1000, 12-station keyboards cost $18.60 (Form A) to $42.50 (Form 2C). For 16-position keyboards, the respective prices are $24.75 and $56.50.—***Tom Ormond***

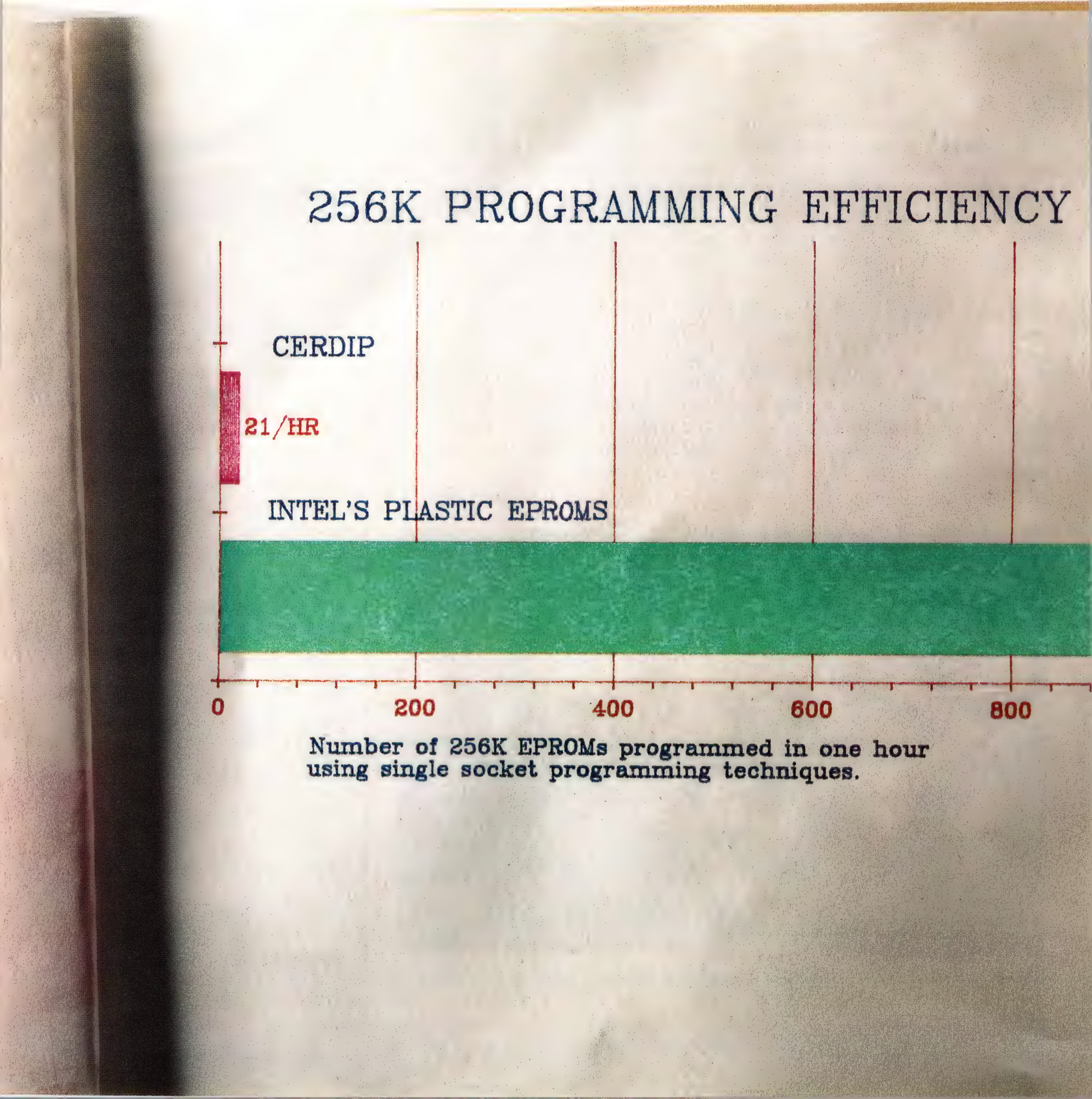
DPI Laboratories Inc, Membrane Technology Div, 359 S Rosemead Blvd, Pasadena, CA 91107. Phone (818) 449-6022.

Circle No 726



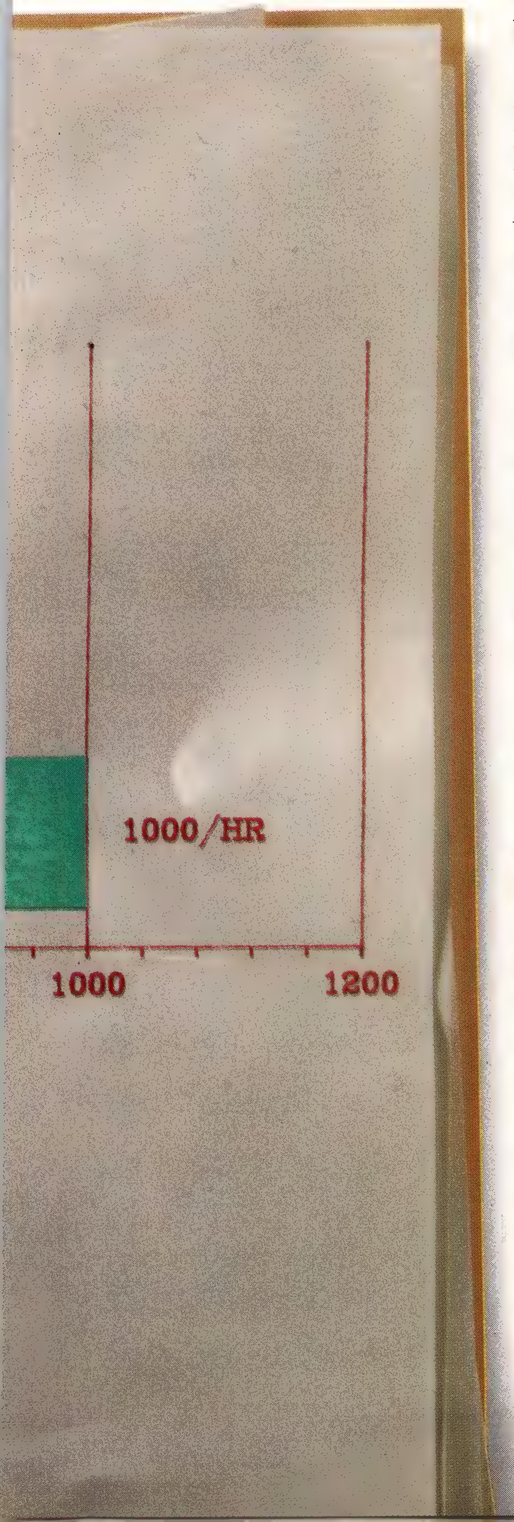
Able to withstand rough environmental conditions, *Series MT-8700 stainless-steel membrane keyboards are available in four different contact configurations. They operate over −20 to +125°C and spec a 3 million-cycle lifetime.*

THE BOTTOM LINE IS THE REASON YOU SHOULD USE OUR NEW PRODUCTION EPROMS.



Study the bottom line and you'll find that now, using Intel's Quick-Pulse Programming™ algorithm, you can program a 27256 plastic production EPROM in less than four seconds. Which translates into 1000 EPROMs in a single hour.

Versus only 21 CERDIP (using conventional programming algorithms).



Which not only saves you time, but saves you equipment and labor costs as well. In fact, you can now program our P27256 EPROM for less than a tenth of a cent.

And because you program so much more quickly, you improve throughput. Getting more product out the door. Which is great for your bottom line.

And since these fast-programming EPROMs are plastic, they're perfect for auto-insertion and high-volume applications. Bringing you one step closer to a fully automated factory.

Our production EPROMs also have a great bottom line against ROMs. Using Intel's new algorithm in tandem with plastic can push the overall cost of EPROMs well under what you pay for ROMs.

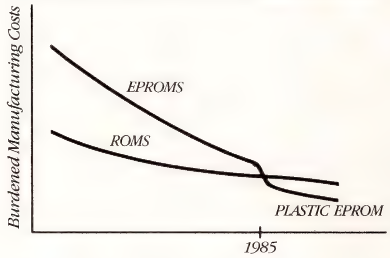
Which means you can stay with EPROMs and never use ROMs again. And never worry about another code change. Or the nightmare of your production line coming to a dead halt. You'll be able to react instantly to market changes. With no wasted inventory. Ever.

You'll also have the superior reliability of Intel production EPROMs.

Intel is the first manufacturer with 100% testing of plastic EPROMs both before and after assembly. And with the same high programmability yield rate as CERDIP. Typically 99.9%. Plus our package reliability surpasses the industry standards for steam and moisture testing.

Best of all, our new production EPROMs with our new algorithm are available now in the quantities you need. And in densities from P2764A through P27256. With programming support from both Intel and Data I/O production gang programmers.

COST-EFFECTIVENESS OF PLASTIC EPROMS ILLUSTRATED



The advent of plastic EPROMs along with Intel's new Quick-Pulse Programming™ Algorithm, has made them more cost effective than ROMs in many applications.

For more information on fast programming, and our new reliability report, call toll-free 800-538-1876, or write Intel Corporation, Lit. Dept. W-248, 3065 Bowers Ave., Santa Clara, CA 95051.

Or better yet, call your local Intel sales office and we'll discuss the cost-saving features of these production EPROMs with you personally.

So you can get right down to the bottom line.

Fast.

intel®

CIRCLE NO 71

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	0	82	18	0	0	9.5	9.7
Pot-Core	0	27	64	9	0	0	7.1	8.5
Laminate (power)	0	31	61	8	0	0	6.8	8.8
CONNECTORS								
Military panel	0	25	50	25	0	0	8.5	10.6
Flat/Cable	5	60	30	5	0	0	4.4	5.4
Multipin circular	6	44	28	22	0	0	6.7	8.8
PC	17	39	33	11	0	0	5.2	4.3
RF/Coaxial	0	50	42	8	0	0	5.7	7.1
Socket	30	44	22	4	0	0	3.3	4.2
Terminal blocks	10	60	25	5	0	0	4.0	4.3
Edge card	0	69	26	5	0	0	4.3	6.2
Subminiature	6	59	35	0	0	0	4.0	6.7
Rack & panel	0	33	67	0	0	0	6.0	6.0
Power	0	55	45	0	0	0	4.7	6.6
PRINTED CIRCUIT BOARDS								
Single-sided	0	50	50	0	0	0	5.0	3.7
Double-sided	0	52	41	7	0	0	5.0	5.3
Multilayer	0	31	53	16	0	0	7.4	7.2
Prototype	8	88	4	0	0	0	2.1	2.7
RESISTORS								
Carbon film	41	41	14	4	0	0	2.5	2.7
Carbon composition	27	50	9	14	0	0	3.9	3.8
Metal film	29	46	21	4	0	0	3.3	3.9
Metal oxide	14	43	43	0	0	0	4.3	3.2
Wirewound	13	48	35	4	0	0	4.4	8.1
Potentiometers	17	37	33	13	0	0	5.4	5.4
Networks	27	27	46	0	0	0	4.2	5.1
FUSES	35	40	25	0	0	0	2.8	2.6
SWITCHES								
Pushbutton	19	48	28	5	0	0	4.0	3.5
Rotary	11	31	42	11	5	0	7.1	4.2
Rocker	0	43	50	7	0	0	6.0	5.3
Thumbwheel	8	33	42	17	0	0	6.7	7.1
Snap-action	17	58	25	0	0	0	3.2	4.9
Momentary	0	67	25	8	0	0	4.7	6.1
Dualin-line	6	69	25	0	0	0	3.4	5.2
WIRE AND CABLE								
Coaxial	35	47	18	0	0	0	2.4	2.5
Flat ribbon	37	47	16	0	0	0	2.2	3.1
Multiconductor	18	59	23	0	0	0	3.1	4.1
Hookup	37	58	5	0	0	0	1.6	1.3
Wirewrap	54	38	8	0	0	0	1.4	1.7
Power cords	26	52	17	5	0	0	3.1	3.8
Other	50	17	33	0	0	0	3.0	6.6
POWER SUPPLIES								
Switching	5	42	37	16	0	0	6.3	8.4
Linear	0	50	37	13	0	0	6.0	6.1
CIRCUIT BREAKERS	20	20	53	7	0	0	5.7	5.8
HEAT SINKS	24	38	33	5	0	0	4.2	3.9

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
General purpose	30	10	50	10	0	0	5.8	4.8
PC board	12	23	53	6	6	0	7.2	6.3
Dry reed	0	50	50	0	0	0	5.0	4.6
Mercury	0	14	86	0	0	0	7.1	6.3
Solid state	15	15	62	8	0	0	6.5	6.4
DISCRETE SEMICONDUCTORS								
Diode	32	35	30	0	0	3	4.0	5.0
Zener	30	33	33	4	0	0	3.9	4.0
Thyristor	13	40	40	7	0	0	5.1	4.2
Small signal transistor	33	24	38	5	0	0	4.3	3.2
FET, MOS	7	47	33	13	0	0	5.7	5.6
Power, bipolar	20	27	53	0	0	0	4.8	5.9
INTEGRATED CIRCUITS, DIGITAL								
CMOS	18	36	32	14	0	0	5.6	5.1
TTL	34	23	35	4	4	0	4.8	5.8
LS	25	43	25	4	3	0	4.4	6.0
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	15	31	39	15	0	0	6.2	6.0
OP amplifier	10	48	28	14	0	0	5.5	5.8
Voltage regulator	14	52	29	5	0	0	4.1	5.0
MEMORY CIRCUITS								
RAM 16k	8	38	46	8	0	0	5.7	5.1
RAM 64k	41	29	30	0	0	0	2.9	4.4
RAM 256k	19	44	31	6	0	0	4.4	5.7
ROM/PROM	14	57	29	0	0	0	3.4	7.2
EPROM	23	38	29	10	0	0	4.6	6.0
EEPROM	15	38	39	8	0	0	5.1	5.7
DISPLAYS								
Panel meters	17	17	58	0	8	0	7.2	5.0
Fluorescent	0	33	67	0	0	0	6.0	6.1
Incandescent	14	14	72	0	0	0	6.0	5.3
LED	11	50	33	6	0	0	4.6	5.3
Liquid crystal	0	12	63	25	0	0	9.3	8.2
MICROPROCESSOR ICs								
8-bit	31	38	31	0	0	0	3.3	6.9
16-bit	19	37	44	0	0	0	4.3	7.9
FUNCTION PACKAGES								
Amplifier	0	44	56	0	0	0	5.3	6.8
Converter, analog to digital	0	40	50	10	0	0	6.4	6.7
Converter, digital to analog	0	25	58	17	0	0	7.8	7.2
LINE FILTERS	0	33	67	0	0	0	6.0	5.4
CAPACITORS								
Ceramic	32	43	21	4	0	0	3.1	5.2
Ceramic monolithic	18	36	36	10	0	0	5.1	4.2
Ceramic disc	40	32	20	4	4	0	3.9	3.5
Film	17	48	26	9	0	0	4.4	4.8
Electrolytic	24	52	16	8	0	0	3.6	5.5
Tantalum	18	41	26	15	0	0	5.3	5.3
INDUCTORS	25	33	42	0	0	0	4.0	4.0

Source: *Purchasing* magazine's electronic business survey

SIEMENS

Graphics Boards for AMS and SMP Systems

A picture is worth a thousand bytes

Alphanumerics displayed on terminals are usually precise and clear but sometimes you need much more.

By compressing large amounts of data into charts, curves or pictures you will obtain a quick overview, recognize changes and trends – you will stay in the picture.

With the new graphics boards 354 the AMS and SMP systems offer a cost- effective solution for such applications. This concept is based on open and standardized hard- and software interfaces. These features assure the future of your system.

Here are the most important characteristics of the AMS-M 354 and SMP 354:

- display formats 1024 by 1024 pixels for AMS and 512 by 512 for SMP
- eight colors
- frame rates up to 70 Hz, non-interlaced
- software driver included in delivery

In addition AMS-specific features:

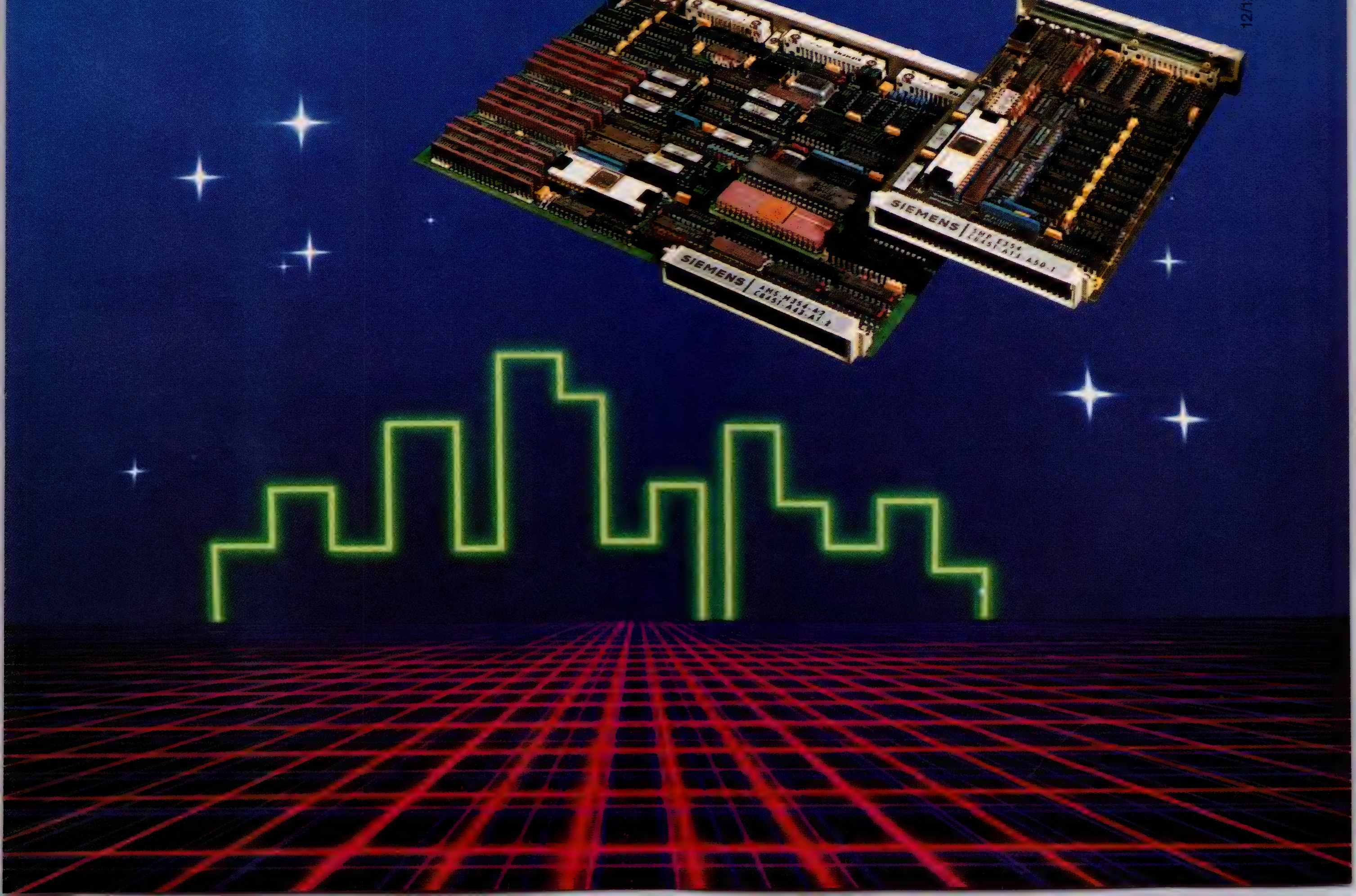
- local processing capabilities, using two 8 MHz processors
- standardized graphics software – the Graphical Kernel System GKS.

For additional information please contact our local Siemens office or Siemens AG, Infoservice 12/1234, Postfach 2348, D-8510 Fürth, "Graphics Board Systems for AMS and SMP".

AMS, SMP, PMS – the Microcomputer Board Systems from Siemens

CIRCLE NO 72

12/1234.101



When the chips are down,

GaAs FETs FROM HARRIS MICROWAVE: YOU CAN'T AFFORD TO WAIT.

You know all GaAs chips are not created equal. . . so when you shop for FETs, you search for the best value. When it comes to performance, quality, service and price. . . Harris delivers.

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Selective ion implantation and in-house material growth provide superior uniformity and wafer-to-wafer consistency. The first ten chips you buy from Harris will perform to the same set of rigid specifications as the chips you purchase six months from now.

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Harris quality certification tests are as rugged as our chips. Each and every Harris GaAs FET wafer must pass a battery of tests which exceed the Element Evaluation requirements of MIL-STD-883C, Method 5008, Class B. And Harris GaAs FET chips are uniquely serialized for the ultimate in traceability.

Harris delivers.

Our complete family of low noise, high gain and power optimized FETs are available *now* from a large inventory of prequalified wafers. On-time customer delivery is our forte.

The best news? Harris FETs are competitively priced . . . and we intend to keep it that way.

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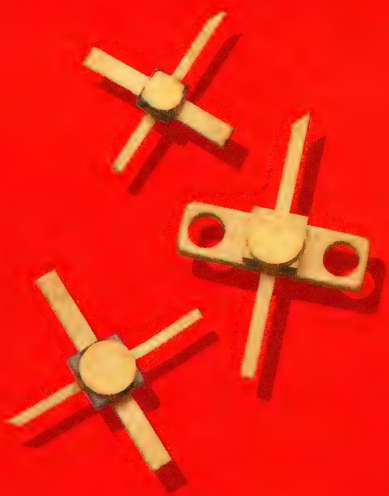
Harris Microwave Semiconductor, 1530 McCarthy Boulevard, Milpitas, CA 95035, (408) 262-2222 (TWX 910 338 2247)

Delivers on time.

GaAs FETs From Harris.



For your information, our name is Harris.

HARRIS

CIRCLE NO 73

Special Report

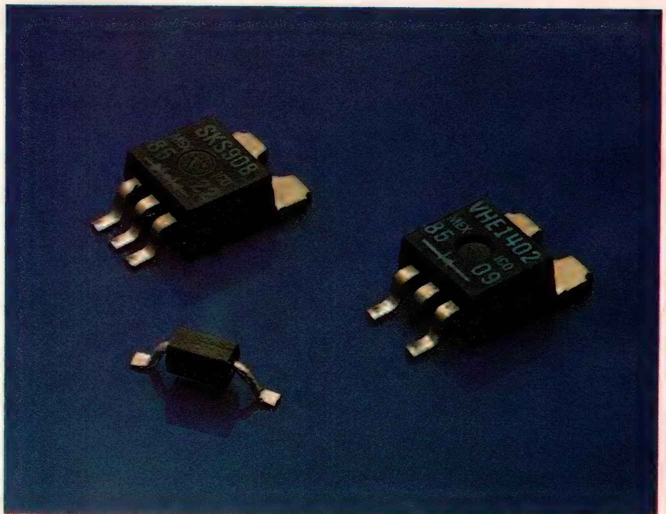
Diodes and rectifiers

Today's high-density systems demand low on-voltages, good thermal properties, and fast recovery characteristics from the diodes and rectifiers used in power-conversion and circuit-protection circuitry. Besides providing these advantages, recent diodes and rectifiers offer volumetrically efficient packaging.

Bill Travis, *Senior Editor*

Driven by demands for improved efficiency in compact systems, manufacturers of diodes and rectifiers are offering products that show improved forward-voltage-drop, turn-off-time, and reverse-voltage capabilities. Such characteristics are important in a variety of applications. Consider, for example, that systems now operate from lower power-supply voltages than they did in the past, and the decreasing power-supply voltages (for instance, from the traditional ±15V to the now ubiquitous 5V to the future 3.3V standard) create a need for efficient, low-drop rectifiers. Further, the growing adoption of high-frequency switching supplies creates the need for rectifiers that combine fast switching and low voltage drop.

As with other electronic products, improvements in diodes and rectifiers (the terms can be interchangeable; a rectifier is simply a high-current—roughly ≥0.5A—diode) come about via improvements in processing and packaging, as well as via the adoption of entirely new classes of devices. Processing advances are responsible for such improvements as lower forward drop, increased reverse-voltage capabilities, and decreased recovery time. Recent packaging innovations improve rectifiers' thermal-transfer characteristics and ease of mounting. And nontraditional devices—for example, a bipolar transistor designed for use as a synchronous



Suitable for pick-and-place mounting techniques, *these small-outline rectifiers from Varo offer current ratings of 1 to 20A and reverse-voltage capabilities of from 20 to 600V.*

Rectifiers' fast recovery times *and low forward-voltage drops let you unlock improved system efficiency, even when you're designing low-voltage circuits. (Photo courtesy Unitrode)*

This isolated module, *Westinghouse's Pow-R-Blok, accommodates various thyristor/rectifier combinations, controls currents as high as 160A per device, and guarantees 2500V isolation. You can obtain the module with single or dual devices.*

rectifier—deliver efficiency that traditional rectifiers can't match.

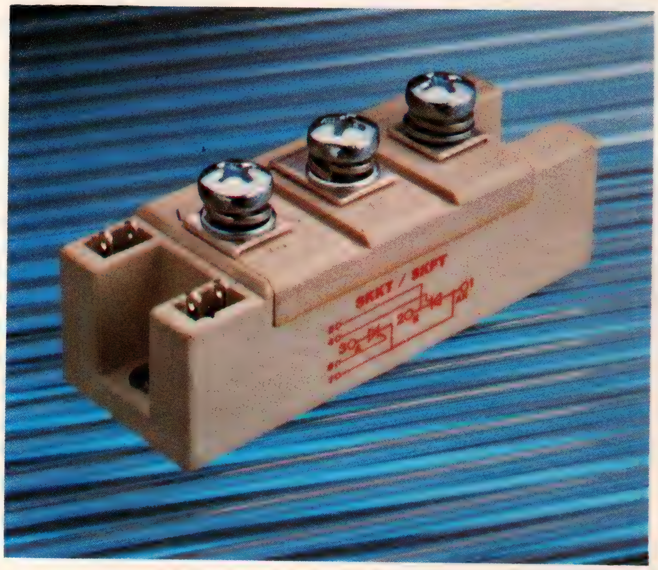
In comparison with pn-junction devices, Schottky rectifiers exhibit much lower forward-voltage drop. For a given current rating, a Schottky unit displays an on-voltage measuring 50 to 70% that of a pn rectifier of comparable die size. The Schottky devices offer considerable advantages, therefore, in systems in which a rectifier's forward drop can compromise efficiency. A prominent example of such systems is a low-voltage switching power supply. Consider, for instance, a 5V, 100A supply in which the rectifiers (pn types) exhibit 1.1V forward drop. You can easily calculate that 110W power loss occurs in the rectifiers. Reducing the forward drop to 0.60V (by using Schottky devices) cuts this power loss to 60W.

Note that, because a Schottky rectifier is a majority-carrier device, it doesn't have a reverse-recovery-time spec. In contrast, a pn rectifier, which works with minority carriers, carries stored charge that's proportional to the current conducted in the forward direction. Reverse-recovery time in such devices is the time required to sweep out these minority-carrier charges. A Schottky rectifier, on the other hand, exhibits a large junction capacitance—for large units, this spec may reach several thousand picofarads.

According to Unitrode Corp (in its Application Note U-85), the high junction capacitance of a Schottky rectifier makes the device's recovery characteristic resemble that of a fast pn-junction rectifier. And, because Schottky devices are prone to excessive heating and damage in the breakdown mode, it's a good idea to use an RC snubber network across the rectifier. The large junction capacitance is the reason that Unitrode, as well as other companies, includes a maximum slew-rate spec (for example, 1000V/μsec) in the data sheets for its Schottky rectifiers. According to the expression i=CdV/dt, the application of a fast-slewing reverse voltage can cause excessive and damaging charging currents to flow.

Unitrode will shortly announce a series of low-V_F Schottky rectifiers. A 25V, 75A (average forward current) model packaged in a DO-5 case operates over −65 to +175°C and specs 0.8°C/W θ_{JC} (junction-to-case thermal resistance). The company also plans to offer the rectifiers in power modules and in a TO-247 (modified TO-220) plastic package. The as-yet-unnamed devices will spec 125°C forward-voltage drops of 425, 450, and 550 mV at currents of 60, 75, and 150A, respectively.

The firm is also reducing forward voltages in its lower-current devices. One example—the $6.45 (100) USD245 4A, 45V rectifier—specs 0.45V max forward voltage at 2A and 125°C junction temperature. The supplier claims the 0.45V V_F is the lowest forward-voltage spec available in the industry. The USD245, which comes in a TO-39 metal can, has 450-pF max junction capacitance and withstands a 1000V/μsec slew rate. According to the manufacturer, the device has a softer recovery characteristic than that of ultrafast



An isolated module with high thermal efficiency, *the Semipack 2 from Semikron can contain rectifiers that control currents as high as 160A and withstand reverse voltages as high as 1800V. The module accommodates any combination of thyristors and rectifiers.*

A Schottky diode's low forward-voltage drop lets you design efficient, low-voltage supplies. Be sure, however, to take the junction capacitance into account.

pn-junction devices. The recovery characteristic is a function of the junction capacitance and the external circuitry (see **box,** "Keep diode recovery time short").

A typical example of DO-5-encased Schottky rectifiers that spec low forward voltages (though not as low as that of the USD245) is the industry-standard SD51, which is produced by Solitron, Varo, Motorola, Unitrode, International Rectifier, and Siemens. This rectifier is a 60A, 45V device that specs 0.6V V_F at 60A, 125°C. Its maximum reverse current is 50 mA at 25°C and 200 mA at 125°C. The device's junction capacitance is 4000 pF max, and its maximum permissible slew rate is 700V/μsec.

For high-current applications requiring low forward-voltage drops, consider a center-tapped, dual-diode assembly from Siemens Colorado Components Div. The common-cathode D2015, intended for full-wave rectification, comes in the company's PowerMod module. The assembly is rated at 25V, 170A (average current) per leg; maximum surge current per leg is 2000A. Forward voltage is 0.46V at 50A, 25°C. The thermally efficient package provides a maximum θ_{JC} of 0.5°C/W per leg, 0.3°C/W per package.

A center-tapped rectifier module from International Rectifier allows you to connect its two internal rectifiers in parallel for an increased current rating. The isolated 161CMQ Series, available in reverse-voltage ratings from 30 to 50V, operates with junction temperatures as high as 175°C. Maximum average output current from the center-tapped network is 160A. Forward voltage is 0.68V at rated current and 125°C junction temperature. Junction capacitance is 2900 pF per leg, and the maximum permitted slew rate for the application of reverse voltage is 1000V/μsec.

To obtain low forward voltages, consider germanium rectifiers as an alternative to Schottky diodes. Although their leakage currents at high temperatures are higher than those of silicon-based diodes, germanium devices offer the benefit of very low forward drop. A series of germanium rectifiers from Germanium Power Devices Corp guarantees 0.5V V_F at currents from 15 to 500A and reverse voltages from 20 to 40V. Although the germanium units' recovery times are only moderately fast (350 to 650 nsec), the devices offer much lower thermal resistivity than do Schottky diodes. Typical germanium rectifiers in DO-4 cases exhibit 0.75°C/W junction-to-case resistivity (θ_{JC}), compared with Schottky diodes' 2°C/W.

Although they clearly exhibit lower forward-voltage specs than do pn-junction devices, Schottky diodes are

Able to control currents as high as 300A, *the Semipack Series Schottky rectifiers from Semikron come in isolated and nonisolated versions. The units spec a 0.8V forward drop at 200A, and they can withstand surge currents as high as 2100A.*

limited-voltage components. In most manufacturers' catalogs, in fact, the upper limits on reverse voltage for Schottky diodes are 45 or 50V. Taking into consideration the normal reverse voltages and the transients that occur in power-supply circuitry, this reverse-voltage limitation all but restricts Schottky rectifiers to 5V (max) power-supply applications. Several manufacturers are, however, taking steps to raise the voltage ceiling.

International Rectifier, another supplier of both Schottky and pn-junction rectifiers, has recently announced a series of 90 and 100V, 1.1A Schottky rectifiers. The 11DQ09 and 11DQ10 (rated at 90 and 100V, respectively) complement the firm's 30, 40, 50, and 60V plastic, axial-leaded devices. Forward drop for both the 90 and 100V rectifiers is 0.87V at 2.2A peak and 25°C. This forward voltage (at a current 2.2 times the average-current spec) compares favorably with that of most ultrafast, 1A pn-junction rectifiers, which spec V_F higher than 0.87V even at the 1A average-current level.

Text continues on pg 132

Keep diode recovery time short

To reduce switching losses, you should keep diode recovery time as short as possible. Understanding the recovery characteristics of the two diode types—pn-junction and Schottky—can help you in your selection and specification of rectifiers.

A pn-junction diode operating in the forward mode contains stored charge in the form of excess minority carriers. If the circuit connected to the diode tries to turn the diode off, as in **Fig Aa,** the stored charge makes the diode appear to be a short circuit during the period t_A **(Fig Ab).** Transition from t_A to t_B occurs when the stored charge is depleted to the point at which it can no longer supply the increasing current demanded by the circuit.

During the transition period t_B, the device presents a high impedance and the reverse voltage is permitted to increase; reverse current dies down as the excess charge approaches zero. The curve in **Fig Ab** is that of a diode with a soft recovery characteristic. An abrupt recovery characteristic is shown in **Fig Ac.** According to Unitrode product manager Vinnie Guercio, a more useful way to specify rectifiers (than using the universal t_{RR} spec) would be to give values for I_{RM}, softness (t_A/t_B), and the area under the t_B portion of the recovery characteristic.

Softness increases losses

To understand why a long recovery time, especially one with a soft characteristic, is deleterious in switching circuits, consider the buck regulator in **Fig Ba.** In this regulator, the transistor's on-time controls the conversion; a control circuit senses the output voltage and controls the transistor's base drive. The inductor current is substantially constant as it flows alternately through the transistor and the catch diode.

The curves in **Fig Bb** show the effects of the diode's reverse recovery time on the transistor's current, voltage, and power dissipation. The broken-line curves represent the performance you'd obtain if the diode had zero recovery time; the shaded area in the transistor's power curve indicates the additional power dissipation attributable to the recovery time. You can see that a

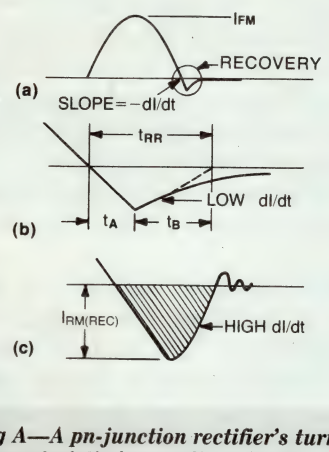


Fig A—A pn-junction rectifier's turn-off characteristic *is complicated, as you can see from these curves. The turn-off current waveform in* ***a*** *follows a JEDEC standard for current slew rate. The turn-off characteristics for soft and abrupt recoveries are shown in* ***b*** *and* ***c****, respectively.*

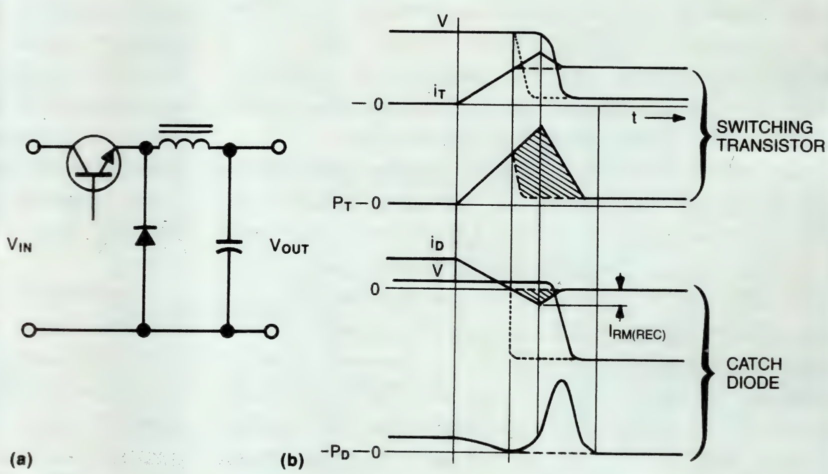


Fig B—A buck regulator circuit (a) illustrates *the losses attributable to a rectifier's reverse-recovery time. The shaded areas in* ***b*** *represent the rectifier's recovery time; you can see that a large part of the loss occurs in the recovery-time interval immediately following the diode's negative-current peak.*

large portion of the losses occurs in the t_B portion of the recovery time; that is, after the recovery characteristic passes the peak negative current $I_{RM(REC)}$.

Paradoxically, because of the losses produced by the diode's recovery time, the use of extremely fast switching transistors doesn't necessarily result in reduced switching losses. Unless you use a diode whose recovery time is two to three times shorter than the transistor's current rise time, the use of a faster transistor will increase the diode's peak recovery current and thus *increase* overall switching losses.

Schottkys vs pn diodes

A popular belief, but one that's only partly true, is that a Schottky diode has no reverse recovery time. It's true that the Schottky's majority-carrier mechanism eliminates the reverse-recovery characteristic that a pn device's minority-carrier storage causes. However, because of the large junction capacitance (about five times that of a junction diode), a Schottky device can exhibit a reverse recovery time equivalent to that of a fast pn-junction rectifier.

To get a feel for a Schottky diode's turn-off effects, consider **Fig Ca,** which depicts an output circuit for a typical switching regulator. Because of the interaction of the transformer's leakage inductance and the diode's junction capacitance, the reverse recovery of the diode assumes a "ringing" aspect, shown in **Fig Cb.** The resonance can, in fact, result in a large enough negative-voltage overshoot to destroy the diode.

The overshoot explains the presence of the RC snubber networks you see connected across the diodes. Without the snubbers, the diode's voltage waveform resembles the one in **Fig Cc;** the addition of the snubbers produces the more tranquil voltage waveform seen in **Fig Cd.**

The material and drawings in this box are adapted from Unitrode Corp's Applications Handbook 1985-86, *a power-conversion design guide that gives detailed design rules and equations for power supplies of virtually every existing topology.*

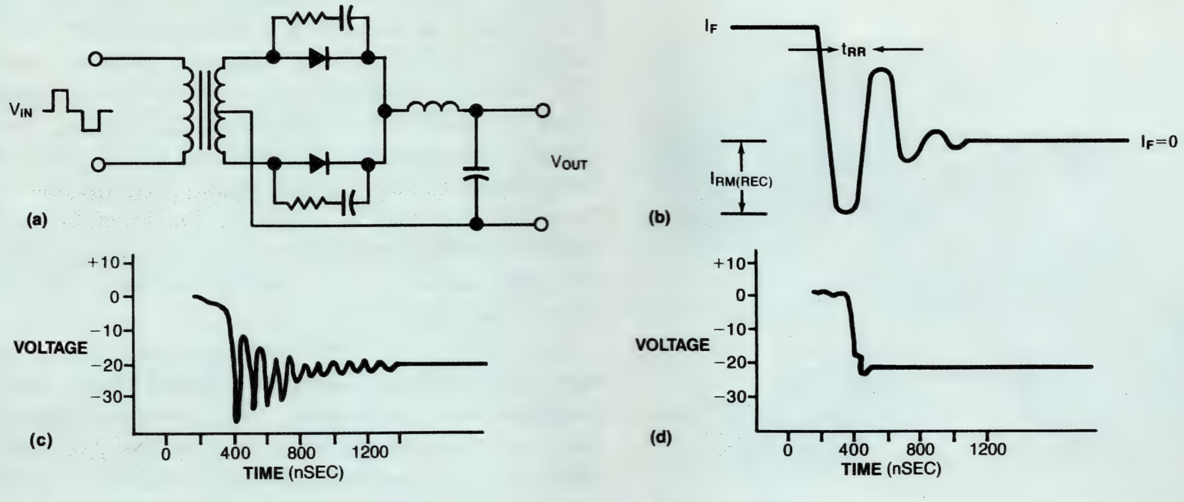
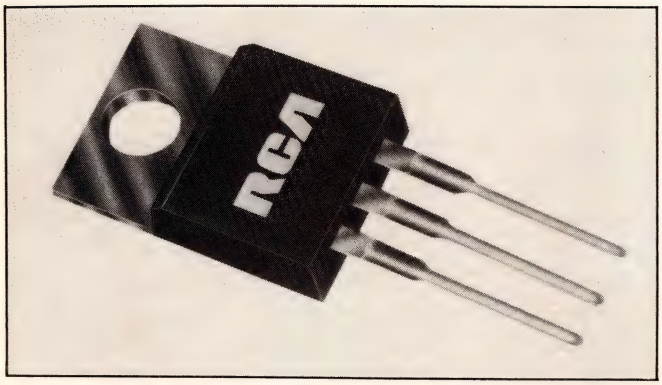
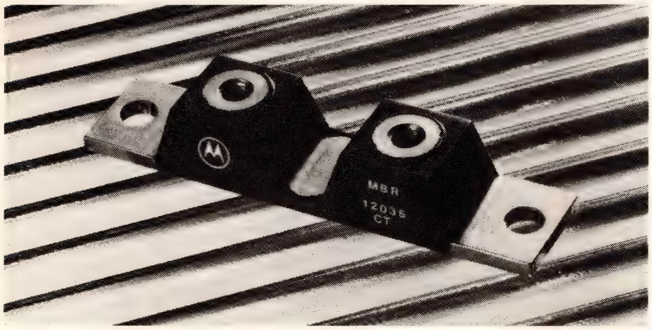


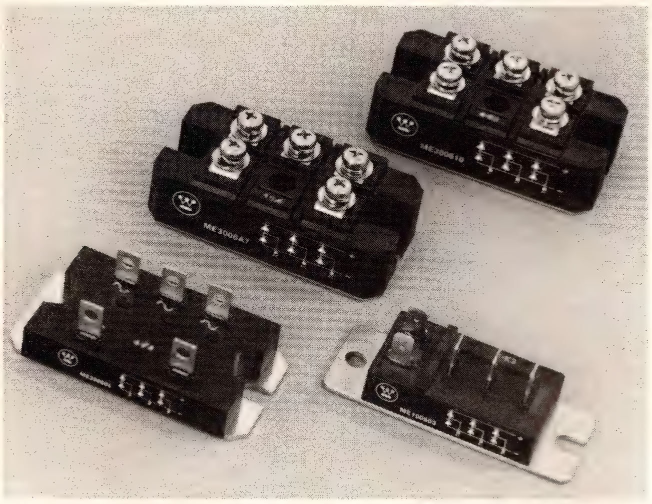
Fig C—A Schottky rectifier's large junction capacitance** can cause trouble in a switching regulator like the one in **a.** Circuit inductance, in conjunction with the diode's capacitance, produces a ringing characteristic **(b).** Unless you use a snubber, the rectifier's voltage waveform also rings wildly **(c);** the snubber eliminates the ringing, which is dangerous to the diode **(d).



This specialized rectifier *from RCA fulfills two roles—that of a normal rectifying diode, and that of a precisely controlled zener diode. Called the load-dump rectifier, it's eminently suitable in automotive applications, in which it's necessary to clamp large, inductively produced reverse voltages.*



Suitable for full-wave rectification, *Motorola's MBR120XX Series dual, center-tapped Schottky rectifiers come in 60 and 100A versions. The XX in the part number designates voltage rating from 35 to 60V.*



Designed for 3-phase rectification, *the Six/Pac Series high-power rectifiers from Westinghouse can control currents as high as 100. The modules offer voltage ratings as high as 1600V, and they can withstand surge currents as high as 1000A.*

Motorola Semiconductor Products is also increasing voltage ratings for its Schottky devices. For example, six recently announced diodes from the company offer reverse-voltage ratings from 20 to 60V. The 60V units are suitable for 12V power-supply applications. Motorola uses a platinum and nickel construction that allows the plastic, axial-leaded rectifiers to spec 3A over −65 to +150°C. Forward-voltage drop for the 20, 30, and 40V MBR320/330/340 is 0.5V at 1A; for the 50 and 60V MBR350/360, it's 0.6V. Prices for the series range from $0.95 to $1.75 (100).

Also targeting 12V power-supply applications, Motorola's MBR1060 is a 10A Schottky device with 60V reverse-blocking capability. The rectifier comes in the TO-220 plastic package. Forward drop for the $1.67 (100) MBR1061 is typically 0.6V at 10A and 100°C junction temperature. Among the company's high-current Schottky rectifiers are four new dual rectifiers that extend their family's previous 40V reverse-voltage limit to 50 and 60V. The units are dual, center-tapped assemblies intended for full-wave rectification. Packaged in the company's PowerTap module, the devices are available in 60 and 100A versions. The 50V, 60A MBR12050CT and the 60V, 60A MBR12060CT cost $21.25 and $23.50 (100), respectively; the 50V, 60A MBR20050CT and the 60V, 100A MBR20060CT cost $29.40 and $34.40 (100).

Semikron offers a line of Schottky-rectifier modules that cover the range of currents from 160 to 300A. Packaged in the firm's Semipack modules, the devices are available in isolated and nonisolated versions. The isolated SKMD-S160, for example, is rated at 160A, 60V; Model SKMD-S200 is a nonisolated assembly rated at 200A, 60V. The manufacturer also supplies special versions rated at currents as high as 300A. Both devices spec a surge-current rating of 2100A; maximum forward drop is 0.8V at 200A. The modules provide top-side screw terminations. The nonisolated units use the base plate as the common-cathode connection. Prices start at $20 (100).

As attractive as Schottky diodes' low forward-voltage drop may be, the laws of physics restrict their use to low-voltage applications. For systems requiring diodes with reverse-blocking capabilities greater than 100V, you must resort to pn-junction devices. Although these diodes don't use radically new technology, manufacturers are continually improving the diodes' electrical parameters, ratings ranges, and thermal-transfer efficiency.

One example of such improvements is Motorola's

The recovery-time characteristics of pn-junction and Schottky rectifiers differ; you must use different design techniques in circuits using these rectifier types.

addition of 700, 800, 900, and 1000V units to its MUR Series, which was previously limited to 600V. The diodes spec 75-nsec recovery time and operate at junction temperatures as high as 175°C. Available in 1A (MUR170/180/190/1100), 4A (MUR470/480/490/4100), and 8A (MUR870/880/890/8100) versions, the devices come in three different packages. The 1A and 4A units are housed in the firm's 59-04 and 267-01 axial-leaded plastic packages, respectively; the 8A rectifier is packaged in the TO-220 plastic case. Prices range from $1 to $2.93 (100).

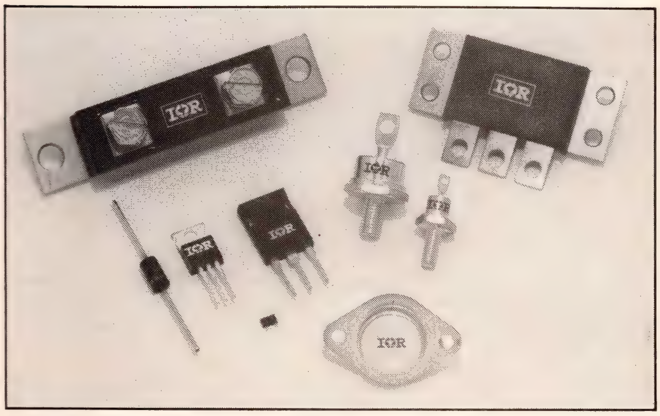
According to Microsemi Corp, its Series 60S and 30S rectifiers are 30% smaller than competitors' equivalent devices. The rectifiers come in two axial-leaded, plastic case sizes. The firm purchased the line from International Rectifier in 1984 to complement its line of zener diodes and rectifiers. The 60S and 30S units are 6 and 3A rectifiers, respectively, and they're available with peak reverse-voltage ratings from 50 to 1000V. The 6A device is capable of withstanding 400A surge current; the 3A unit, 150A surge.

A series of axial, diffused-junction rectifiers from diode manufacturer RSM Sensitron Semiconductor offers a choice of 70- or 100-nsec recovery time. The 70-nsec series comprises the S320S7, S330S7, and S340S7, whose peak inverse-voltage ratings are 200, 300, and 400V, respectively. Models S320S10, S340S10, and S360S10 withstand reverse voltages of 200, 400, and 600V, respectively, and spec 100-nsec recovery time. The rectifiers are rated at 3A at 55°C and 2A at 100°C. Forward-voltage drop at 3A is 1.25V for the 70-nsec units, 1.5V for the 100-nsec devices.

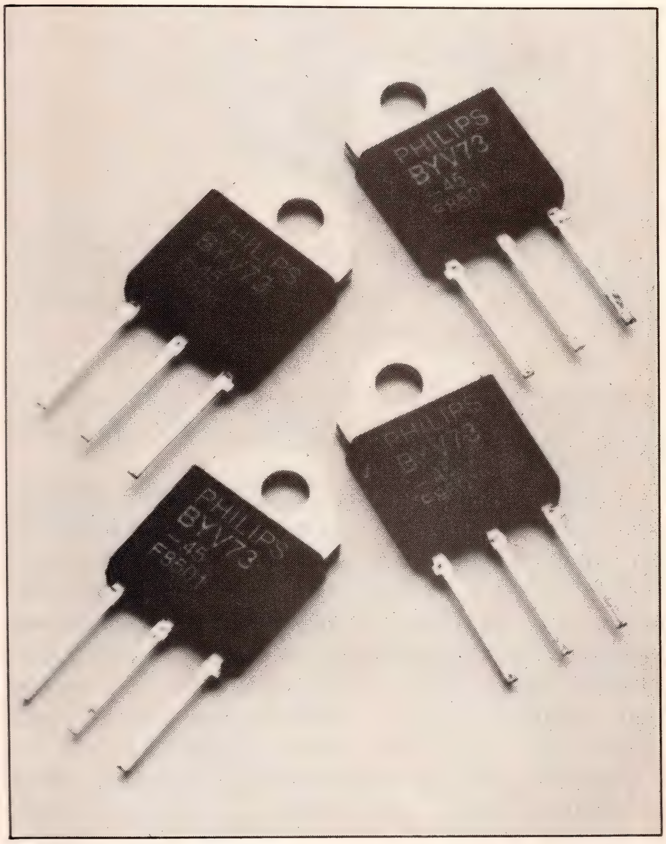
Power assemblies

Manufacturers of high-power rectifiers are also seeking ways to pack more function into a given volume. Several recent offerings represent improvements in volumetric efficiency. Volumetric efficiency, in this case, means thermal efficiency—it's important both for a rectifier assembly to be able to handle a great deal of power in a given package and for a package to conduct heat away from the rectifiers efficiently.

A family of isolated, 3-phase (six diodes) rectifier modules from Westinghouse Electric Corp allows designers to shrink the size and cost of inverters commonly used in uninterruptible power supplies, ac-motor speed controllers, and servo systems. The Six/Pac modules come in 12 rating combinations—four current ratings (30, 50, 75, and 100A) and three voltage ratings (600, 1200, and 1600V). The modules withstand large



***Available in a wide variety of packages** from miniature to large, Schottky rectifiers from International Rectifier satisfy a wide range of system needs. From left to right, the two top devices are a molded Schottky module and a low-profile power Schottky assembly. In the second row, the packages are an axial type, a TO-220, a TO-3P (TO-247), a DO-5, and a DO-4. The two bottom devices are a surface-mount Schottky diode and a TO-3 unit.*



***Profiting from the TO-218's impressive thermal properties,** these dual Schottky rectifiers from Amperex control 30A per device and spec reverse voltages of 30 to 45V. The 1-chip construction allows you to connect the two diodes in parallel without spec derating.*

Signal diodes, rectifier diodes, and zener diodes *come in these cylindrical, surface-mountable packages from Rohm Corp. The signal and rectifier diodes meet all specs of the ubiquitous 1N4148 and 1N4001 families.*

A series of cylindrical, glass-passivated rectifiers *from General Instrument offers current ratings of 1 and 3A and specs reverse voltages as high as 1000V. The units are available with recovery-time specs from 50 to 500 nsec.*

overcurrents—for example, units rated at 100A have a surge-current capability of 1000A. The price for a 75A, 600V module is $46 (10).

Another example of improved ratings is Westinghouse's Pow-R-Blok modules, whose previous 40/60/90A ratings have been raised to 130 and 160A. The single- and dual-device modules spec 2500V isolation. For applications requiring hermeticity, the company can incorporate ceramic-encased rectifiers in the modules. The firm claims that its compression-bonded encapsulation technique imparts optimum heat-transfer and temperature-cycling characteristics to the modules.

Rectifier and thyristor manufacturer Semikron offers an isolated, 2-diode module that has a surge-current rating 25% higher—for the assembly's package size—than is available elsewhere, the firm claims. This 160A module, Semipack 2, fills the gap between the manufacturer's Semipack 1 and 3 modules, which are rated at 90 and 250A, respectively. Offering screw-terminal connections on its top side, the unit has the same mounting-hole pattern (80 mm center-to-center) as the Semipack 1 and 3 devices. The module can withstand 5100A surge current. It specs 2500V isolation voltage and is available with reverse-voltage ratings as high as 1800V. A 130A, 1200V assembly with a 1000V/μsec dV/dt rating costs $85 (200).

A series of modules called Magn-A-Pak from International Rectifier also offers high-current ratings in a package that has a small footprint. The isolated-base module measures 3.62×1.97×2.05 in. and comes in 1- or 2-diode configurations. Other available configurations include a double thryristor and a thyristor/diode pair. The diodes, which offer current ratings as high as 260A, withstand surge currents as high as 8500A and current slew rates to 800A/μsec. All modules undergo isolation testing to 2500V rms. A single-diode Magn-A-Pak module rated at 200A and 800V costs $256.50 (50).

A convenient configuration for full-wave rectification is the single-phase bridge **(Fig 1a)**, which contains four diodes connected in series. Note that the configuration also can help protect battery-powered circuits: You can connect a battery in either polarity to the bridge's ac terminals, and the bridge's positive and negative terminals will always apply the correct polarity to the load.

Several manufacturers are making strides in the ratings and volumetric efficiency of these assemblies. Consider, for example, the Slimline Series of bridges from RSM Sensitron. These bridges come in low-profile cases that present low thermal impedance to the internal rectifiers. The SL6300, SL1500, and SL30300 bridges are available with reverse-voltage ratings of 1000V in the general-purpose (5-μsec recovery) version and 600V in the fast-recovery (150 nsec) version. The SL1500 and SL30300 also come in a 150V, 30-nsec version. The SL1500 is a single-phase, 15A assembly that has 2°C/W thermal impedance and 0.31-in. case height. A 3-phase **(Fig 1b)** version with 0.25-in. case height, the SL6300, also specs 2°C/W thermal impedance. The 30A SL30300, another 3-phase assembly, specs 1.25°C/W thermal impedance and comes in a case that's 0.31-in. high. Prices for 200V, general-purpose versions range from $20 to $44 (100).

Two more bridges complete the spate of recent offerings from RSM Sensitron. For military applications, both are available with internal JAN, JANTX, or JANTXV hermetically sealed diodes. The 3-phase S35A300 offers higher power ratings than do standard, similarly packaged MIL-standard M19500/483 bridges. The series is rated at 35A continuous and 250A surge—

Schottky rectifiers' increased voltage ratings permit the design of efficient 12V power supplies and allow for wider safety margins in designs.

ratings that are 10 and 100A higher, respectively, than those for standard M19500/483 bridges. Peak inverse-voltage ratings for general-purpose (5 μsec), fast-recovery (150 nsec), and ultrafast (30 nsec) versions are 1000, 600, and 150V. A 200V, general-purpose unit costs $60 (100). General Instrument also offers MIL bridges; its recently introduced M19500/469 assembly is rated at 10A. The company offers 200, 400, 600, and 800V versions for $14.28 (100).

Another bridge offering improved volumetric efficiency (as compared with other currently available bridges) is the single-phase S30A05HE Series from RSM Sensitron. The device is also available with internal MIL-standard diodes. The manufacturer claims that the bridge delivers 65% more output power than other available units while exacting a size penalty of only ⅛ in. in additional length and width. Rated at 33A output current at a 55°C case temperature, the assemblies come in ultrafast, fast, and general-purpose versions having voltage ratings of 150, 600, and 1000V, respectively. An ultrafast (30-nsec recovery) unit rated at 50V costs $72 (100).

Electronic Devices Inc offers two ultrafast (50 nsec) assemblies priced at $2.25 (100). The BRUS-2 Series has wire leads and is rated at 10A; the BRUS-2F offers quick-connect terminals and a 12A rating. Both bridges are available with voltage ratings from 50 to 600V, and both withstand 125A surge current. The assemblies come in a 0.3-in.-high case measuring 0.89 in. in diameter; the case presents a typical θ_{JC} of 5.1 °C/W for the wire-lead version and 4.3°C/W for the quick-connect type.

One example of advances in volumetric efficiency (and, thus, in thermal efficiency) is a series of high-power bridge rectifiers from Semikron. These isolated bridges have a 1.9×2.5-in. footprint and offer ratings of from 40 to 100A at inverse voltages ranging to 1600V. Their case has a 2500V isolation-voltage rating. Available in single- and 3-phase versions, the assemblies meet UL requirements for creep and strike distances for line voltages as high as 600V. Prices start at $22.60 (1000).

The trend toward surface mounting and the need to pack more power into a given volume are giving rise to the development of new packages for diodes and rectifiers. Diode manufacturers have responded to these industry demands for denser packaging by introducing several families of devices that offer a high power/volume ratio.

Generally speaking, surface-mount packages fall into

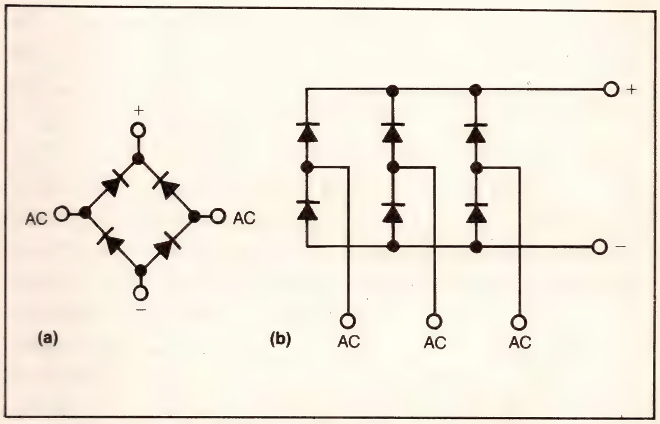
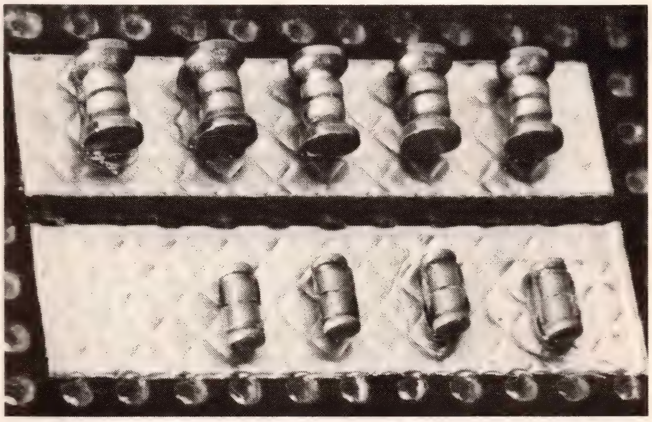
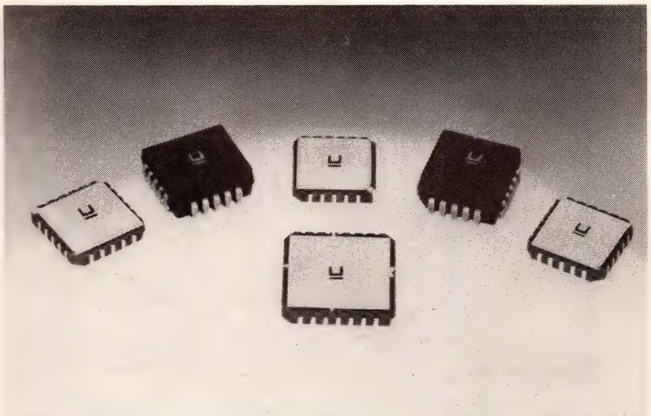


***Fig 1—Building better bridges** is the preoccupation of several semiconductor manufacturers. Such assemblies are available in single-phase **(a)** and 3-phase **(b)** configurations.*



***A new series of cylindrical,** surface-mountable rectifiers, the MELF Series from Unitrode Corp, will accommodate both pn-junction and Schottky versions. All diodes are hermetically sealed and use internal metallurgical bonds.*



***A thermally efficient, surface-mountable package,** the PCLCC from Unitrode Corp, will house the company's complete line of pn-junction and Schottky rectifiers, as well as bipolar and power-MOS transistors.*

Thermally efficient packaging helps pn-junction rectifiers to tolerate the losses attributable to their high forward voltages.

three categories: cylindrical, pellet-type devices; SO (small-outline) plastic units; and traditional TO-220, TO-218, and TO-247 cases with leads cut and formed for surface mounting. In the first category, a wide range of cylindrical, glass-passivated devices comes from General Instrument. The rectifiers offer voltage ratings from 50 to 1000V and current ratings of 1 and 3A. Recovery-time specs range from 50 to 500 nsec. Another source of cylindrical, surface-mount diodes and rectifiers is Rohm Corp, which recently announced a series of industry-standard types, including the ubiquitous 1N4148 signal diode, the 1N4001/4002/4003 family, and a series of zener diodes. The signal, rectifier, and zener diodes cost $0.045, $0.07, and $0.06 (10,000), respectively.

SO-type plastic devices are exemplified by recent offerings from International Rectifier and Varo Semiconductor. Housed in a SOT-89 package, the 10JQ Series from IR is a family of single, 1A Schottky rectifiers that have voltage ratings from 30 to 100V. Maximum forward voltage at 25°C is 0.56V for the 30V units and 0.86V for units rated at 100V. Junction capacitance for the 30 and 100V devices is 60 and 35 pF, respectively. Varo also offers SO-type diodes and rectifiers; the units have ratings ranging from 20 to 600V and 1 to 20A. Both single and center-tapped dual rectifiers are available.

Unitrode Corp will soon announce a broad series of ultrafast (35- and 50-nsec) and Schottky rectifiers in the thermally efficient TO-247 package. The TO-247 is similar to the TO-218 except that it has an all-plastic case with a screw hole; the TO-218 has a metal heat-sink tab. Unitrode's ultrafast rectifiers (available as singles and center-tapped duals) offer current ratings of 16, 30, and 45A and voltage ratings from 50 to 400V. The Schottky devices cover the same current ranges and spec voltage ratings from 20 to 45V.

An example of rectifiers in the TO-218 package is the BYV73 Series, a family of dual Schottky devices rated at 30A (both diodes conducting) from Amperex, a Philips company. The rectifiers, which are available

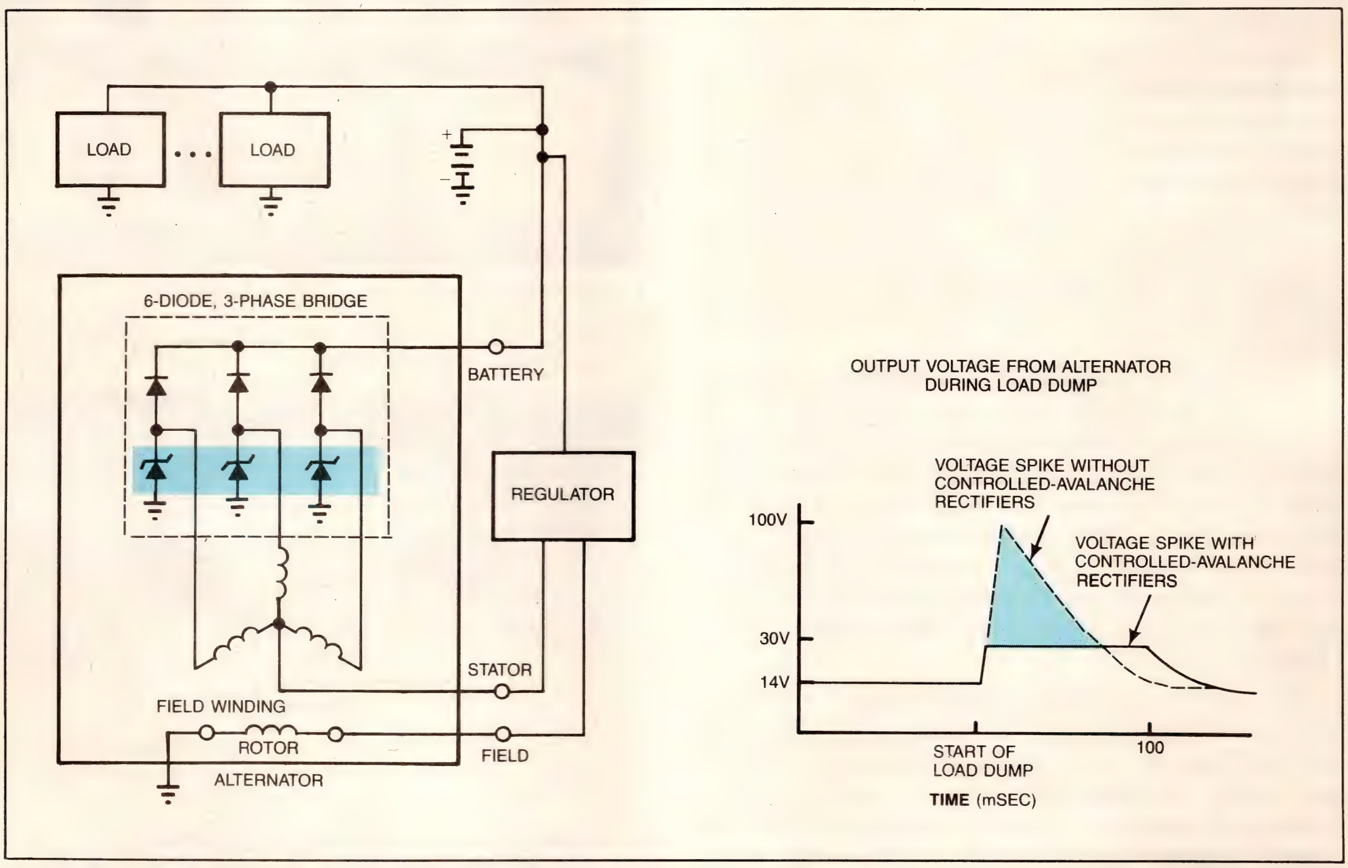


***Fig 2—To suppress inductively induced voltage spikes** in an automotive alternator system, a load-dump rectifier from RCA provides a precisely controlled 30V clamping level. The devices serve two roles: normal rectification and transient suppression.*

Manufacturers of diodes and rectifiers

For more information on diodes and rectifiers, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

AEG Telefunken Corp
Rte 22, Orr Dr
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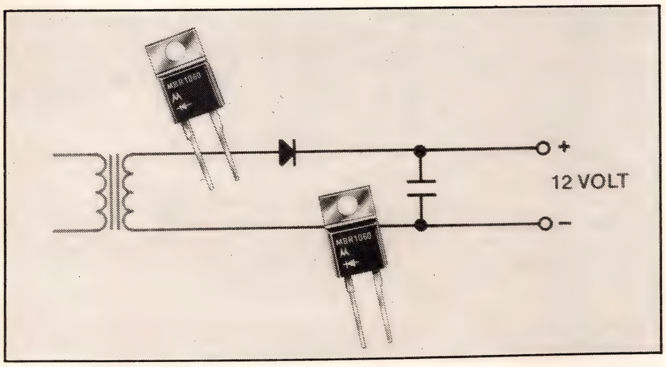
New packaging technology increases rectifiers' thermal efficiency and makes the devices easier to mount in power-control and -conversion circuitry.



Housed in the TO-220 package, *the MBR1060 Schottky rectifier from Motorola specs 60V reverse-blocking capability. The 60V rating makes the units suitable for application in 12V power supplies.*

with voltage ratings of 30, 35, 40, and 45V, each use a single monolithic chip which, the manufacturer claims, ensures near-perfect matching of the two internal diodes. This matching allows you to use the two rectifiers in parallel without incurring any derating. Forward-voltage drop is specified at 0.6V max at 15A, 100°C and 0.87V max at 30A, 25°C junction temperature. Prices for the units range from $3.18 to $3.75 (100).

You can expect a series of innovative, surface-mount rectifiers soon from Unitrode Corp. The MELF Series comprises a family of cylindrical, hermetically sealed units. The series, which will include the firm's full line of pn-junction and Schottky diodes, will come in three sizes: 150 mils in length, 66 mils in diameter; 175 mils in length, 100 mils in diameter; and 210 mils in length, 160 mils in diameter. Each unit will incorporate a metallized bond to the internal chips.

The PCLCC (power ceramic leadless chip carrier) from Unitrode is a hermetic packaging development that serves military and other high-reliability applications. The devices come in two package sizes: 300 and 450 mils square. The smaller size serves applications requiring ratings as high as 10A, 200V; the larger has ratings to 25A, 500V. The larger package's thermal resistance ranges from 0.9 to 2.2°C/W, depending on die size. The company plans to offer its line of pn-junction and Schottky rectifiers, as well as bipolar and power-MOS transistors, in the PCLCC. You can also expect to see some center-tapped dual diodes and quads (either separate or in bridge configuration).

Finally, consider the simplest package of all—none. Solitron Devices Inc offers a series of rectifiers in bare-chip form; the devices have aluminum metallization on top and chromium-silver (for solder mounting) on the bottom. The rectifiers come in ratings from 50 to 500V and withstand surge currents from 30 to 700A.

Just as certain systems call for application-specific ICs, so certain applications demand special rectifying devices. Two examples of such devices are a power-surge suppressor that RCA will soon announce and the BiSyn synchronous rectifier from Unitrode Corp. The first device, which RCA also calls a "load-dump" rectifier, is a controlled-avalanche rectifier that offers precisely controlled reverse-avalanche characteristics.

Intended for use as the output rectifiers in the 3-phase, 6-diode bridge assembly of an automotive alternator **(Fig 2)**, the load-dump rectifier breaks down at a voltage between 24 and 32V. The diodes assume a dual role in this application: They serve as normal forward-clamping rectifiers, and they act as transient suppressors that prevent an automobile's inductive spikes and field-decay transients from damaging electronic circuitry. The firm plans to offer the load-dump rectifiers in TO-220 and -218 plastic cases, as well as in chip form. Current ratings for the rectifiers will be as high as 100A (average forward current).

The second device, Unitrode's UBS430 BiSyn synchronous rectifier **(Ref 1)**, answers the need for low forward drop in low-voltage power supplies (such as the imminent 3.3V-standard supplies). The rectifier is an npn bipolar transistor that specs equal forward and reverse voltage ratings. The firm specifies the UBS430's forward-voltage drop in terms of on-resistance. For example, at 30A forward current, the on-resistance is 10 mΩ max. This value yields 0.3V forward voltage—a voltage far lower than that attainable with any conventional rectifier.

At lower currents, the synchronous rectifier's forward-voltage drop is even lower. At 10A, for example, the drop is only 0.1V, an impressive spec that ordinary rectifiers can't match. The sychronous rectifier can, therefore, contribute to significant yield improvements in low-voltage supplies. For example, the power loss attributed to a Schottky rectifier in a circuit using a 3V load is about 20%. The BiSyn reduces this loss to less than 10%. Housed in a TO-204AE (similar to TO-3) metal case, the 40A, 50V device costs $10 (100). **EDN**

Reference

1. Patel, Raoji, "Bipolar synchronous rectifiers cut supply losses," *EDN*, April 4, 1985, pg 199.

Article Interest Quotient (Circle One)
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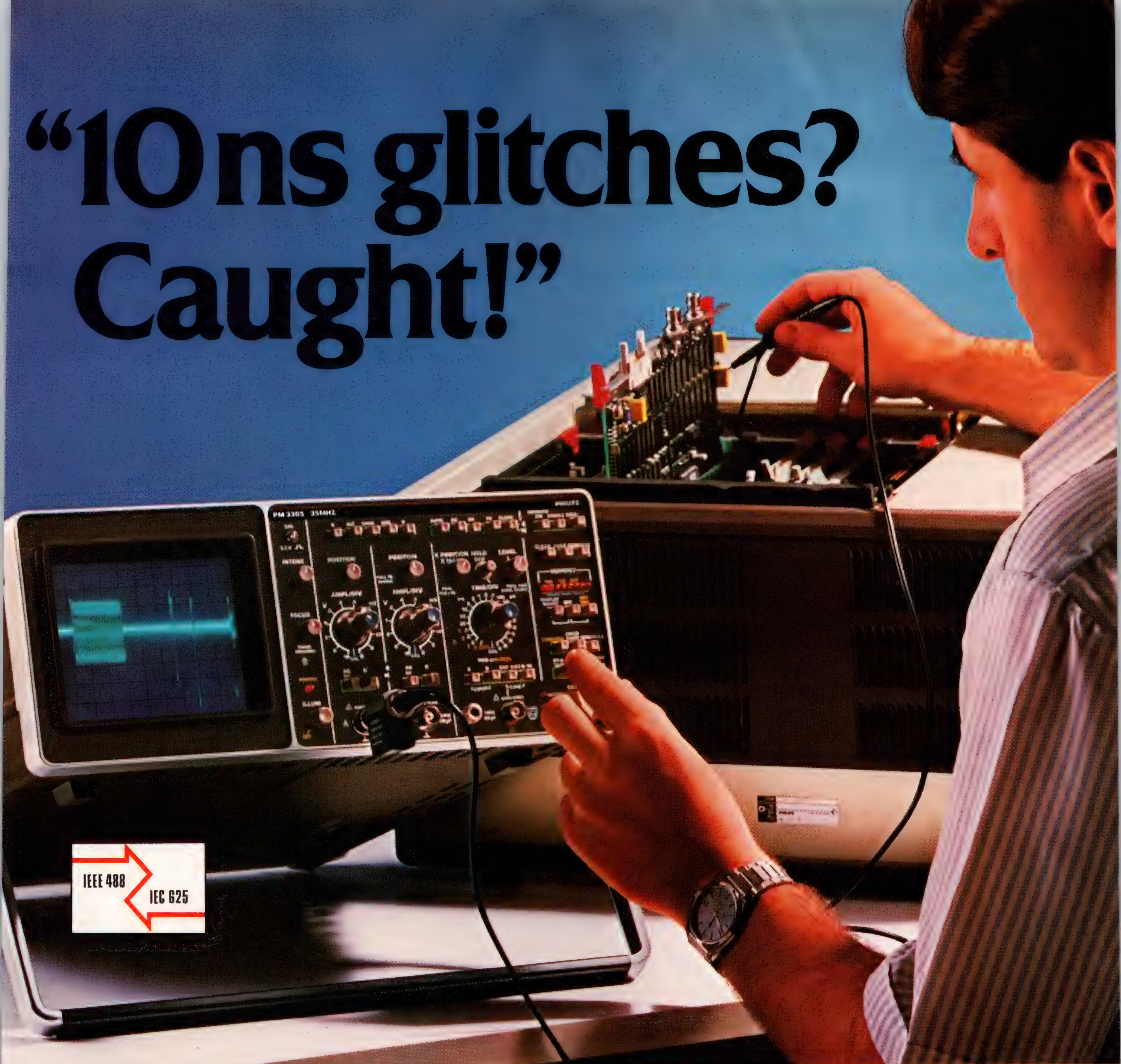

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Instrumentation amp addresses power-miser circuit applications

For many applications, designers are now demanding greater IC performance at lower supply-voltage and -current levels. One monolithic instrumentation amplifier can help satisfy these needs. It's an easy-to-use, self-contained precision gain block that can address isolation and other problems.

Justin McEldowney, *Burr-Brown Corp*

Designers can take advantage of the high performance available in the INA102 monolithic instrumentation amplifier to handle a host of applications where low power consumption is critical. Typical examples of such applications include remote monitoring stations powered by batteries or solar cells, mobile battery-powered circuits, medical instrumentation, remote transducer amplifiers, pulsed control systems, and data-acquisition systems.

Solving isolation problems

Fig 1 shows several designs that exploit the INA102's low current requirements to achieve high-performance isolated data acquisition. **Fig 1a** shows a generic data-acquisition circuit in which the INA102 interfaces directly with a 3656 module, a unit that combines an isolation amplifier with an isolated switch-mode power supply. The transformer-coupled 3656 features a continuous isolation-voltage rating of 3500V dc.

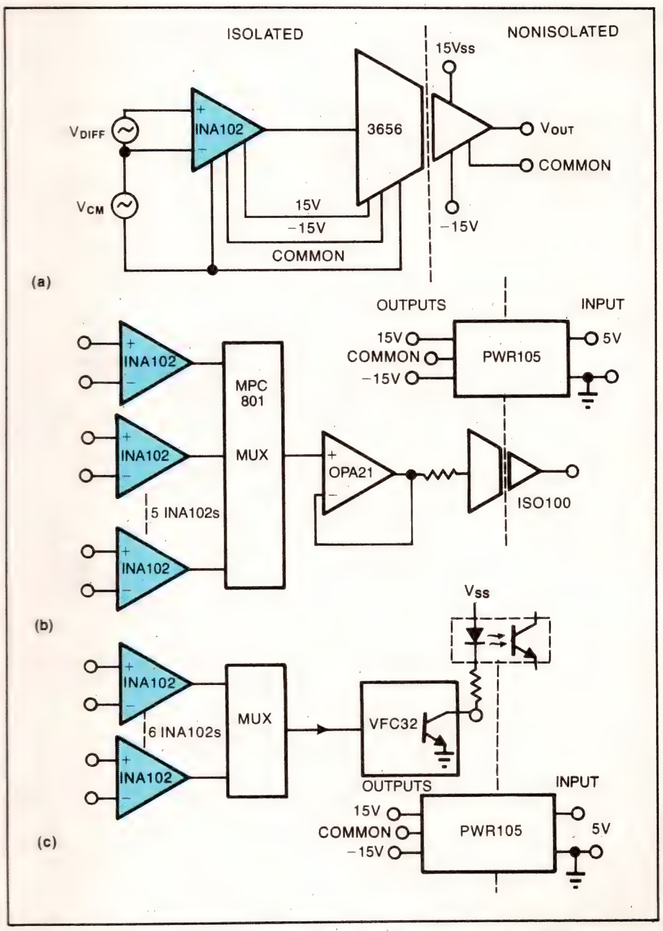

Fig 1—You can achieve high-performance isolated signal acquisition *by exploiting the INA102's low current requirements. You can interface the INA102 directly to an isolation amp **(a)** or an 8-channel CMOS multiplexer **(b)**. Another circuit **(c)** provides an easy technique for analog-to-digital conversion.*

A variety of designs can exploit the INA102's low-current requirements to achieve high performance in isolated data-acquisition circuits.

In **Fig 1b**'s circuit, a separate minisupply drives an 8-channel system. Power requirements for the circuit's CMOS multiplexer are minimal, and the OPA21 op amp draws less than 300 μA. The ISO100 isolation amplifier requires only 75 mW, so total power drain on the isolated power supply is only 325 mW. The PWR105 dc/dc converter operates with a 5V input and delivers ±15V at 15 mA per channel. The ISO100 employs optical coupling. Its peak continuous isolation-voltage rating is only 750V, so it's not as expensive as the 3656.

The circuit shown in **Fig 1c** satisfies applications specifically involving digital signals. The desired channel signal feeds a voltage-to-frequency converter. The V/F converter's output signal is a series of pulses, each of which has a period that's proportional to the input signal. Typically, these pulses are fed to a gated counter to retrieve the original input value.

Although **Fig 1c**'s circuit employs a PWR105 isolated power supply, the output power is a function of the V/F converter you use. If you elect to use the system clock to drive the V/F converter, you can use a VFC100. In this case, you'll need an additional digital optical coupler to drive the VFC100's clock input. If synchronization isn't a major concern, you can use a converter like the VFC32. In either case, the full-scale frequency (dynamic range) is dependent on the speed of the optocouplers.

If high performance isn't a prime design parameter, you can develop an inexpensive but effective isolation amplifier by modulating the current in an optocoupler (**Fig 2**). In this case, the INA102 operates as a high-side current monitor; it's powered by a miniature switch-mode power supply, and it floats on the high voltage input of a motor-drive circuit.

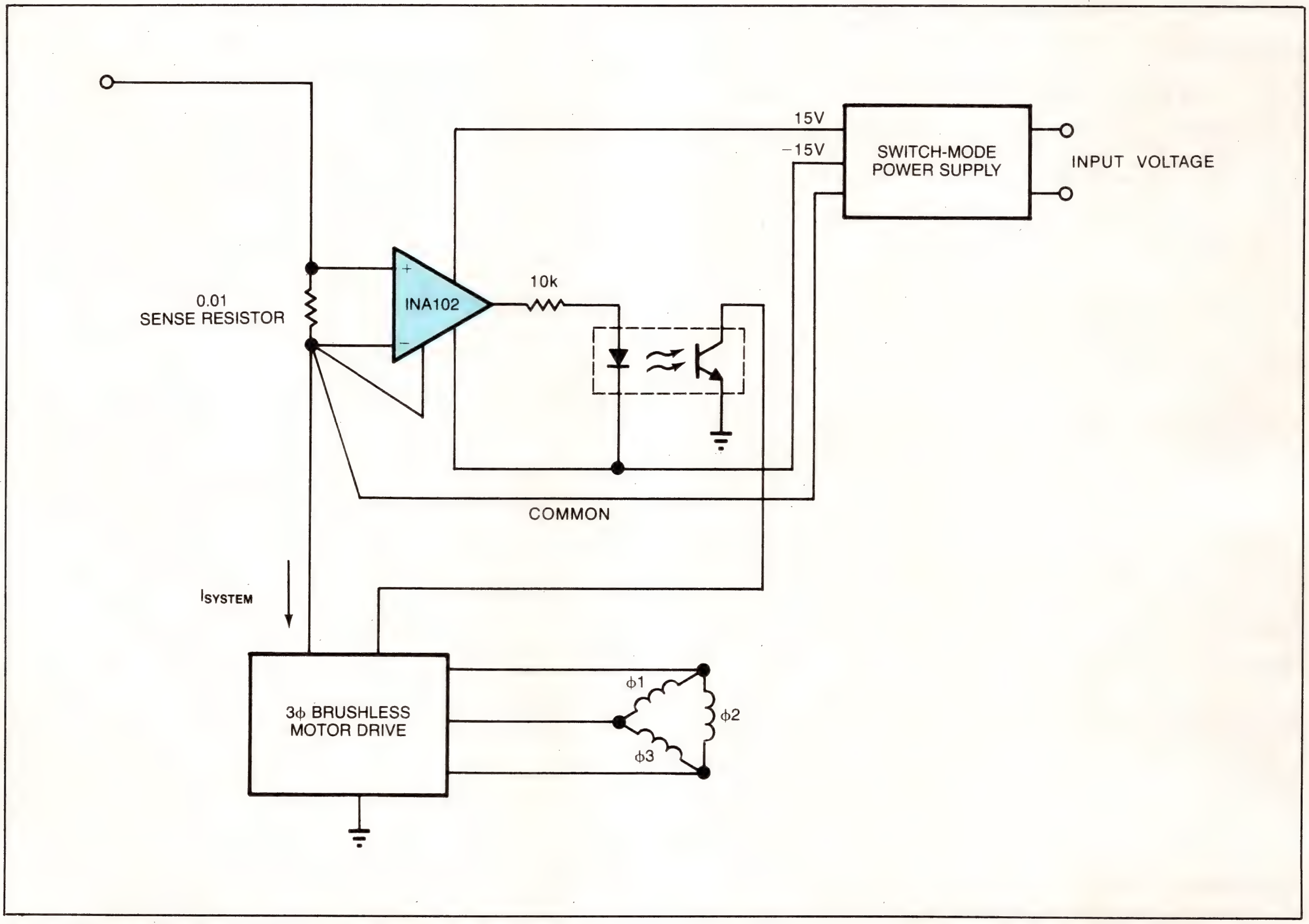

Fig 2—If high performance isn't a prime design parameter, *you can develop an inexpensive but effective isolation amplifier by modulating the current in an optocoupler.*

The high-side current-monitoring concept is important in this design. A sense resistor in the return path (employed in low-side monitoring) would not detect a short from the motor windings to the motor housing, which is usually grounded. If your design employs a 0.01Ω sense resistor, you can read the monitored current directly as the output voltage of the instrumentation amp if the amp's gain is set for 100.

Although the scheme presented in **Fig 2** is quite simple, its precision is not very high. Most optocouplers have a linearity error of about 2%. In addition, the output signal will have an inherent midscale offset that isn't well defined unless you do some trimming. This offset does offer one advantage, however: It allows you to monitor the negative current pumped back into the power supply by the motor.

No discussion of isolation techniques would be complete without a description of a medical-instrumentation application. **Fig 3** illustrates a battery-powered, multichannel EEG system that's clocked by low-power CMOS circuits. These circuits continuously sweep through the channels. The first channel (pin 4) has a 10-kHz square-wave input that identifies channels. This example illustrates a typical application challenge: the measurement of small signals (about 100 μV p-p) from high-impedance sources with as much as 1V p-p of a 60-Hz common-mode signal. Using 15 INA102s, this circuit will draw only 12 mA, including a 1-mA current draw for the CMOS circuitry.

Save power in process monitoring

Many control schemes don't require continuous monitoring of the process. Samples taken at a regular interval (once per second, per minute, etc) suffice. You

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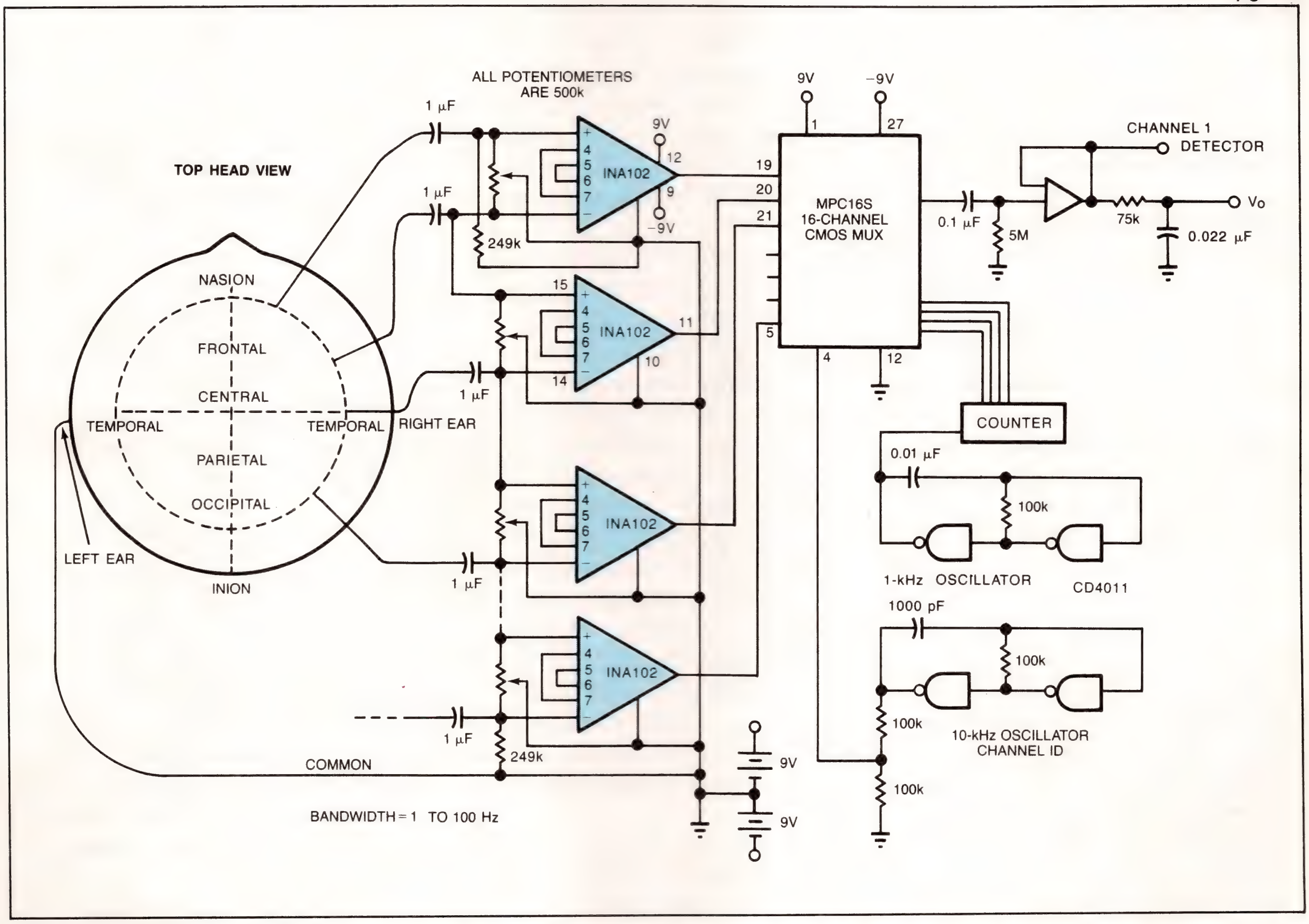


Fig 3—In this battery-powered EEG system, *low-power CMOS circuits provide the clock function and also continuously sweep through the channels. The circuit employs 15 INA102s and draws only 12 mA.*

Choosing an instrumentation amplifier

The best way to do a worst-case amplifier comparison is to analyze all possible error sources. To do so, however, you must be sure that the data sheets you're relying on use consistent units. The most popular error-spec units are parts per million (ppm) per full-scale input and percent of full scale (%FS).

Most of the data-sheet specs are referred to the input. If they're listed in terms of the output, you can refer the figure to the input by dividing by the gain of the amplifier.

Three types of error sources

You can divide error sources into three categories: gain errors, offset and rejection errors, and noise errors. The total noise and nonlinearity of the amplifier will determine the overall signal resolution. Offset and gain-error drifts with temperature will mostly limit the reading accuracy. You can often design around certain error sources (common-mode errors and power-supply ripple, for example), and you can null (or at least account for) most voltage offsets. **Fig A** models the various error sources for an instrumentation amplifier.

The input voltage source (V_D) is the signal you would like to amplify accurately. Unfortunately, the gain equation includes some error components—dc-gain error, gain drift, and gain nonlinearity. Spec sheets usually list dc-gain error in percentage units. However, you must take care to determine gain at the frequency of interest, because gain rolls off after the amplifier's cutoff frequency.

Gain drift is usually listed in ppm/°C, so you have to multiply the figure by the expected operating temperature range to determine the gain drift referred to the input. Gain nonlinearity is also usually given in ppm/°C, and you simply add this error source to the other figures.

Always some residual V_{CM}

V_D is usually riding on some type of common-mode voltage (V_{CM}). Instrumentation amplifiers are designed expressly to reject this common-mode signal, but it will always generate a small output.

Error source V_R combines the effects of the common-mode and power-supply rejection ratios (CMRR and PSRR; both are much smaller than unity). Most monolithic circuits have excellent power-supply rejection, and you can often ignore this source of error. It can be significant in cases where the supply is not well regulated, however. The common-mode rejection ratio is a function of frequency, and you'll have to check the amplifier data sheet to determine the correct value to use in any analysis. Characteristic PSRR curves are usually similar to the CMRR curves.

There are actually two parts that compose the offset voltage (V_{OS})—input offset and output offset. For reference to the input, V_{OS} is easily grouped and modeled as a single voltage source in series with one of the inputs. V_{OS} has both initial and temperature-dependent parts.

Check change in temperature

Input bias currents induce other offset voltages, but they are often negligible. The input offset current is simply the difference between the two input bias currents. R_S represents the Thevenin resistances seen from each input terminal, and ΔR_S signifies the difference between input source impedances. Though several factors contribute to worst-case offset voltage that can be traced to bias currents, the change in operating temperature is the only significant error source.

Thermoelectric effects at the pins of the amplifier package can create other offset errors. These offsets are most severe when there is a temperature gradient across the package.

One more error source

Noise is the final amplifier error source. Other than 60-Hz ground loops, the major sources of noise are shot noise, popcorn (or burst) noise, flicker (or 1/f) noise, and thermal noise. Manufacturers' data sheets usually combine these noise sources into three categories: 1/f noise, noise floor (white noise), and current noise.

Current noise is generally

negligible for bipolar inputs, and you need only multiply the square root of the system bandwidth by the value of the floor-noise density (listed on the data sheet) for the desired gain. You can often use a crest factor of 6.6 to convert the rms value to a 0.1%-probability peak-to-peak value that you can expect to see in any given application. Dividing the 1/f noise by this crest factor will allow you to convert back to an rms value.

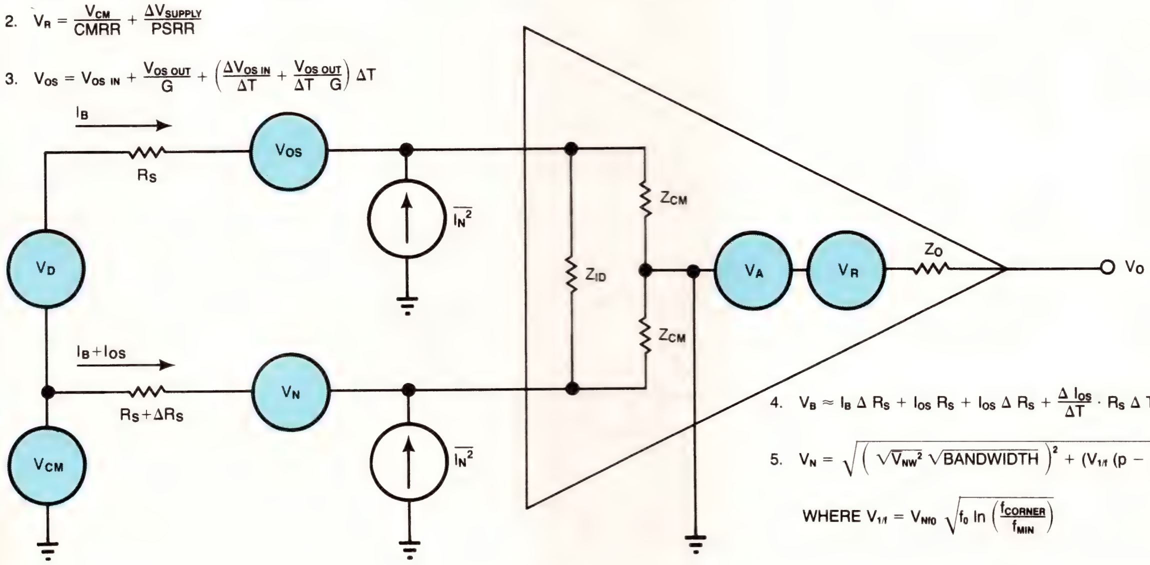
To determine the maximum achievable resolution, you'll need to know the noise floor, the system's bandwidth set by the amplifier or filtering, and the 1/f noise (usually given for 1 to 10 Hz). Note that the equation for noise voltage assumes that the two noise components are uncorrelated, and that it combines them by taking the square root of the sum of their squares. For example, using the INA102 with gain set for 100 and a 1-kHz bandwidth, the input-noise graph on the data sheet shows a 1/f noise figure of 65 nV/$\sqrt{\text{Hz}}$ at 1 kHz. In the 1/f range of 1 to 30 Hz, the flicker noise is 370 nV rms (see **Fig A, Eq 6**). You'll also need the white-noise value: 30 nV/$\sqrt{\text{Hz}}$ × $\sqrt{(1000-30)}$, which equals 934 nV. These figures combine to give 1-μV rms noise referred to the input. With a gain of 100, you can expect to see 100 μV rms at the output. Using a crest factor of 6.6, you'll observe 660 μV p-p on an oscilloscope. With the 20V full-scale output, 660 μV translates into 33 ppm.

The noise-analysis calculation method outlined above is not a rigorous approach; it makes full use of typical amplifier characteristics and provides only approximate results. However, the method does provide a basis for quickly comparing instrumentation amplifiers from different manufacturers.

1. $V_A = V_D$ [GAIN + GAIN ERROR + (GAIN DRIFT × TEMPERATURE CHANGE) + GAIN NONLINEARITY]

2. $V_R = \frac{V_{CM}}{CMRR} + \frac{\Delta V_{SUPPLY}}{PSRR}$

3. $V_{OS} = V_{OS\,IN} + \frac{V_{OS\,OUT}}{G} + \left(\frac{\Delta V_{OS\,IN}}{\Delta T} + \frac{V_{OS\,OUT}}{\Delta T\ G}\right)\Delta T$



4. $V_B \approx I_B\,\Delta R_S + I_{OS}\,R_S + I_{OS}\,\Delta R_S + \frac{\Delta I_{OS}}{\Delta T}\cdot R_S\,\Delta T$

5. $V_N = \sqrt{\left(\sqrt{V_{NW}^2}\sqrt{BANDWIDTH}\right)^2 + (V_{1/f}\,(p-p) \div 6.6)^2}$

WHERE $V_{1/f} = V_{Nf0}\sqrt{f_0 \ln\left(\frac{f_{CORNER}}{f_{MIN}}\right)}$

6. $V_O = V_A + V_R + V_{OS} + V_B + V_N$

Fig A—You can best compare instrumentation amplifier performance *by analyzing all possible error sources. Note that gain and drift errors are referred to the input. V_{NW} is the white-noise magnitude in the white-noise region; the 6.6 divisor in* ***Eq 5*** *is a crest factor that converts a 0.1%-probable peak value to rms.*

If your isolation design doesn't require very high performance, you can build a suitable isolation amp by modulating the current in an optocoupler.

can realize significant power savings by designing a circuit that pulses on for a brief time and then powers down until it's time to take the next sample.

The INA102 is well suited to this type of application. Because of the amplifier's low power requirements, the amount of warm-up heating is very small, and the warm-up time and drift therefore don't compromise performance each time the circuit turns on. Assuming a 70°C/W thermal resistance for a side-brazed ceramic package, the INA102 heats itself less than 2°C, which translates to a worst-case offset warm-up drift of 14 μV. Warm-up time is well under 1 msec. The overall time to acquire a reading after the power comes on will depend both on the time constant of the output filter used to set the system bandwidth and on the settling time of the INA102.

Fig 4 shows an example of this type of application. The example could be a handheld instrument with a simple momentary switch to trigger a reading. The two one-shots fire when the switch closes. The first one-shot turns on a pair of CMOS switches; the second triggers the A/D converter to take a reading. After a reasonable amount of time—determined by the warm-up time, the settling time, and the converter's conversion time—the first one-shot turns off. The resulting measurements might go into a memory or to an LCD. Overall time spent in the power-on mode can range from 1 to 10 msec. At a rate of one sample per second, this circuit can be a real battery saver.

Place dedicated INA102s before mux

The INA102 can also be beneficial in multichannel data-acquisition systems by allowing you to achieve higher throughput rates. Standard data-acquisition systems generally use a multiplexer, located before the instrumentation amplifier, to monitor several channels.

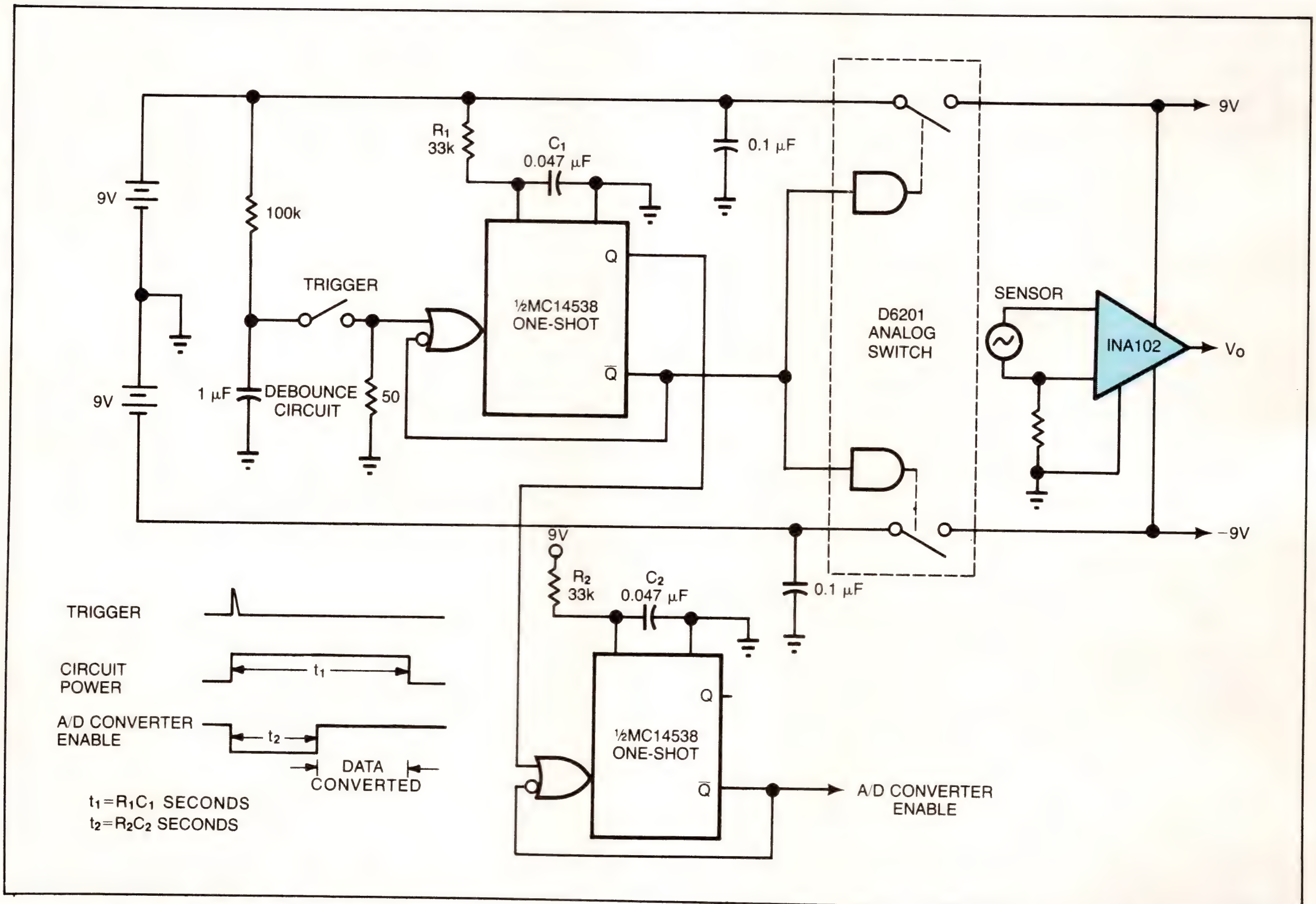


Fig 4—To provide significant power savings *in process-monitoring applications, this circuit pulses on only when it's time to take a sample measurement.*

An EEG application illustrates the challenge of measuring small signals from high-impedance sources with as much as 1V p-p of a 60-Hz common-mode signal.

Such design schemes are used to avoid the high costs of using dedicated instrumentation amps on each channel. These costs include the expense of the extra power, the external components, and the extra system board space required to accommodate the dedicated amps.

You can realize a major increase in performance at a reasonable cost by using dedicated INA102s at each analog input of a data-acquisition system (**Fig 5**). This configuration gives you several dedicated input channels that together require the same power needed to operate one of the older instrumentation circuits. All necessary gain-setting resistors are built in, and users can select the desired gain via jumpers. According to this dedicated concept, the signal is amplified earlier in the system, creating a better signal-to-noise ratio. However, the primary reason for using dedicated input amps is to be able to scan the inputs at a faster rate.

It's important to understand how it's possible to achieve the improved scan rate. No matter which data-acquisition scheme you use, you'll have to reduce your bandwidth in order to reduce input noise. If you use a band-limiting filter, the settling time for signal

The inside story

The INA102 consists of a difference amplifier and a pair of noninverting amplifiers, which buffer the signal at each input (**Fig A**). With all the gain at the input, the signal is amplified prior to encountering the noise inherent in the difference amplifier and the rest of the system.

All the gain-set and difference resistors are laser-trimmed to provide accurate ratio matching. It is this ratio matching that provides the high common-mode signal rejection (90 dB min) and gain accuracy (0.05 to 0.5%, depending on gain). Having all the resistors physically close to each other allows them to track well with changes in temperature, which leads to low gain-drift performance (±5 to ±20 ppm/°C, depending on gain).

Other key specs include a ±3.5 to ±18V supply voltage range, 0.5-mA typ current drain, worst-case linearity error (gain=1000) of 0.05% at 25°C, and an offset voltage of ±300±300/G μV, where G equals gain. Bias current and offset-voltage drift spec 30 nA max and ±2+5/G μV/°C, respectively. Operating temperature range spans −25 to +85°C.

The INA102's gain-setting resistors are not trimmed to an exact value; rather, they are trimmed until their ratios with the feedback resistors have the correct value. Note that the feedback resistor of amplifier IC_2 comes out to a pin rather than to the amplifier's inverting input. This scheme decreases the gain errors by referring wire-bond and pin-contact resistance to the feedback resistor instead of the lower-valued gain-setting resistor. And it doesn't take much stray resistance to create problems. If INA102 gain is set at 1000, 0.2Ω in series with the gain-setting resistor will cause a 0.5% gain error. IC_2 senses the gain-setting resistor without including the error caused by the feedback current and the contact-resistance combination.

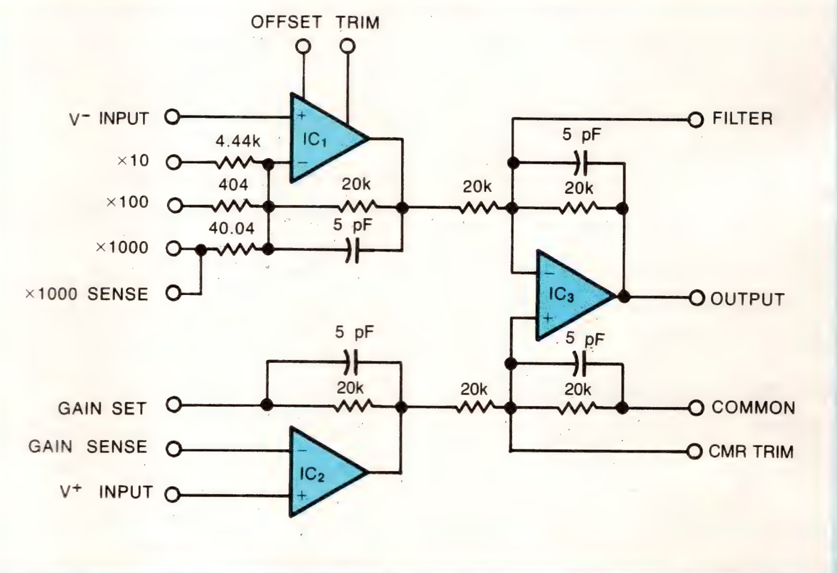


Fig A—The INA102 consists of a difference amplifier and a pair of noninverting amplifiers, which buffer the signal at each input.

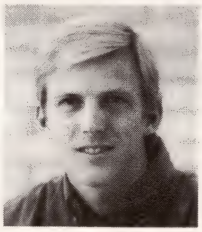
Many control schemes do not require continuous process monitoring; samples taken at regular intervals will suffice.

acquisition will increase. It takes approximately seven time constants for a single-pole filter to settle to 0.1% of its final value. For the 100-Hz-bandwidth filters shown in **Fig 5,** this period comes to almost 11 msec. You must therefore achieve a higher scan rate through the careful choice and placement of other components.

Typical sample/hold circuits can settle in just a couple of microseconds, and most successive-approximation A/D converters will also have finished their task of digitizing the input signal in a few microseconds, so these components add no significant amount of time to the sampling process. The critical factor is the placement of the instrumentation amps with respect to the multiplexer. With the more standard approach of using the multiplexer in front of the instrumentation amplifiers, you can expect a throughput rate of only 93 samples per second; by placing the dedicated INA102s in front of the multiplexer and thereby eliminating the effect of the instrument amps' settling time, you can approach 30,000 samples per second.

Your present power supply is probably adequate to power a 64-channel system. With 64 INA102s operating from a dual 15V supply, power consumption will be about 2W. The INA102 runs cool, so you can increase the circuit board's package density and still not have to employ a fan. **EDN**

Author's biography



Justin McEldowney is an analog circuit design engineer at Burr-Brown Corp (Tucson, AZ). He is currently serving as a project engineer for the design of a new voltage-to-frequency converter. Justin has a BSEE degree from the University of Arizona and is a member of the IEEE. In his spare time, he enjoys backpacking, bicycling, skiing, woodworking, gardening, and cooking.

Article Interest Quotient (Circle One)
High 473 Medium 474 Low 475

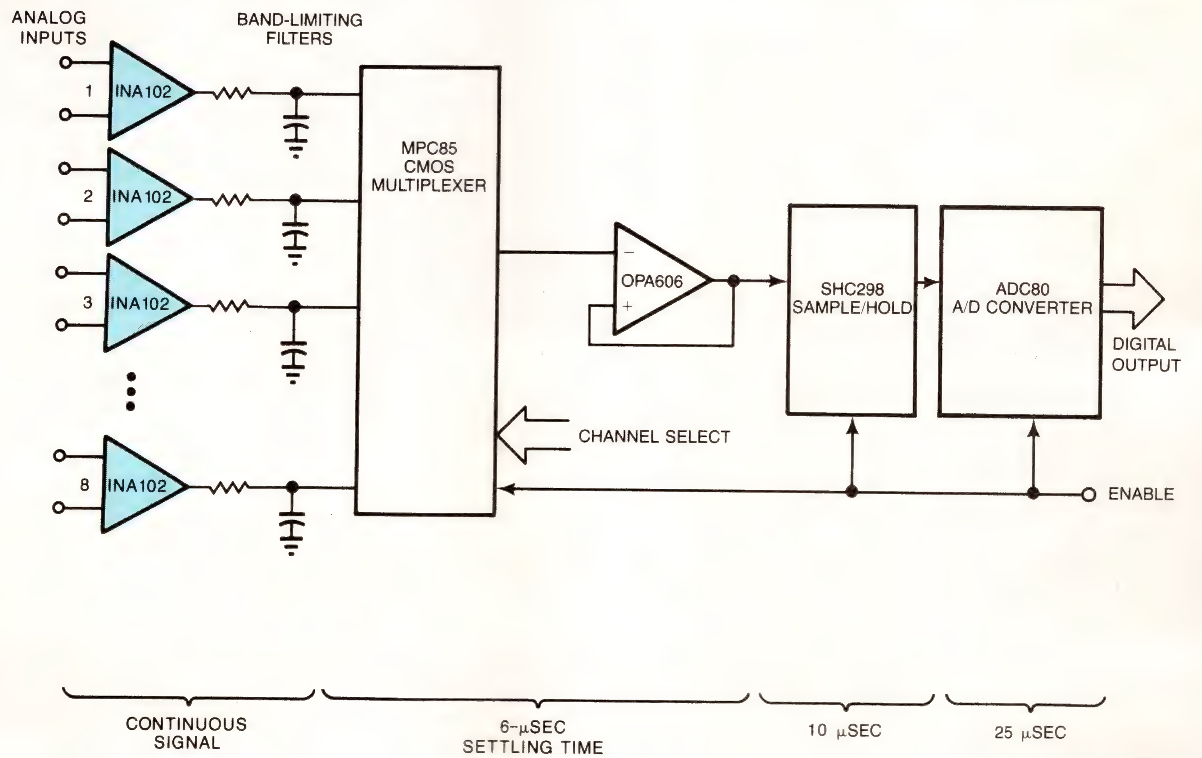


Fig 5—You can increase the throughput rate *of a data-acquisition system by dedicating an INA102 to each analog input channel. In this example, rates can approach 30,000 samples per second.*

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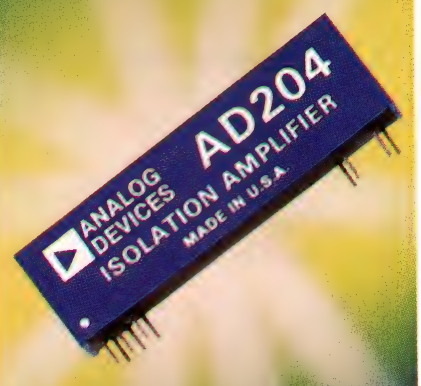

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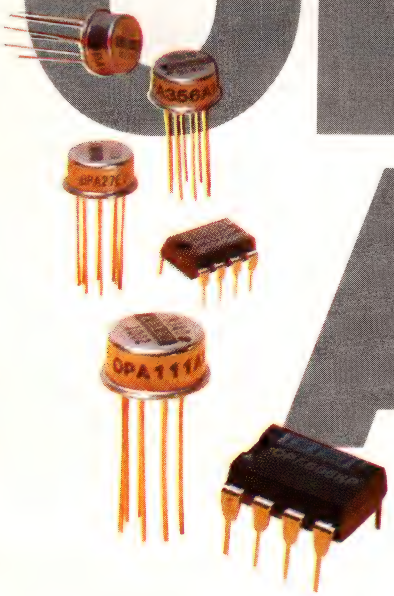

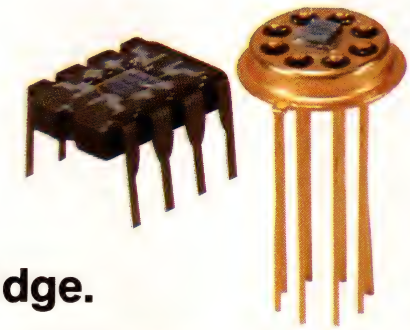

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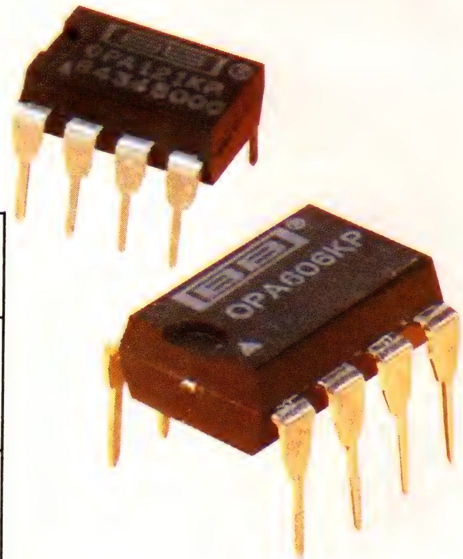

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OPA156A/356A	50pA max bias current at 25°C ambient; 5μV/°C drift; 4MHz min gain bandwidth; 10V/μsec min slew rate.
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ECL technology suits high-speed logic systems

Because they drive low-impedance transmission lines directly, ECL circuits offer both performance and design advantages over Schottky TTL circuits. By using ECL circuits in your high-speed systems, you can eliminate some of the time-delay and distortion problems inherent in such systems.

Kenneth Chan, *Monolithic Memories Inc*

When you design a high-speed logic system, consider using emitter-coupled logic (ECL) circuits as an alternative to Schottky TTL circuits. ECL circuits switch about two to three times faster than do Schottky TTL circuits. Besides its performance advantages, ECL technology offers a number of advantages for the logic-system designer: Its differential output amplifiers, open-emitter outputs, large fan-out, and versatile drive capabilities save both design time and pc-board real estate. Further, by using ECL circuits in your system design, you can minimize some of the common problems associated with high-speed logic circuitry.

Schottky TTL circuits and ECL circuits employ different modes of operation. Like standard TTL, Scottky TTL operates in the saturated region of the transistors' basic current-voltage curve. The base region accumulates carrier electron charges during the transistors' on time and releases them during the transistors' off time. This charge-discharge sequence creates a storage-time delay—a characteristic common to all saturated-type logic circuits.

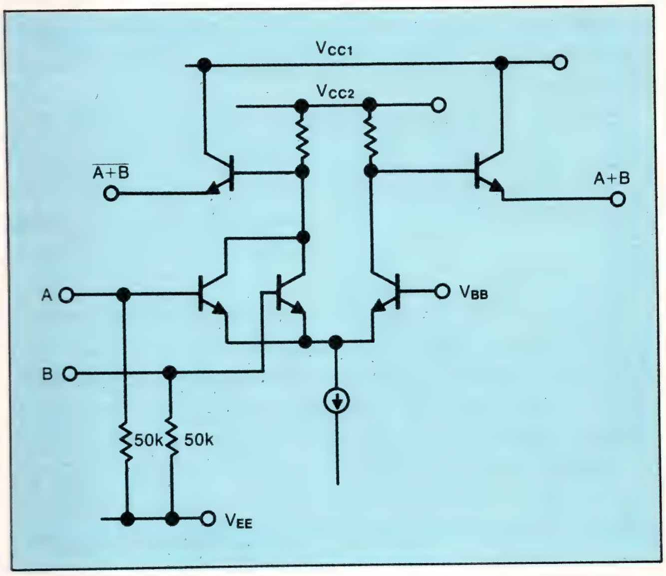


Fig 1—To eliminate output-level fluctuations *caused by supply-voltage variations, connect voltage-supply line V_{CC2} to system ground.*

A Schottky diode clamp between the transistor's base and collector speeds up the discharge process. This technique shortens the discharge delay, but increases input capacitance. On the average, Schottky

Because ECL circuits operate in a nonsaturated mode, they don't exhibit storage-time delays.

TTL circuits can achieve a switching speed of 2 to 3 nsec per gate.

Unlike Schottky TTL circuits, ECL circuits operate in the unsaturated mode, so they don't experience storage-time delay. An ECL transistor can, therefore, achieve a switching speed of 750 psec to 1 nsec per gate—roughly two to three times faster than a Schottky TTL device's switching speed.

Minimize output-level fluctuations

ECL circuits also let you minimize output-level fluctuations and noise on the ground line. **Fig 1** shows the basic configuration of an ECL 2-input OR/NOR gate. The emitter-follower outputs in an ECL gate are derived from the high-voltage supply line, so, by connecting the supply line to the system ground, you can eliminate output-level fluctuations caused by supply-voltage variations.

As a result, the logical one state in ECL circuits is at ground potential and logical zero is at a negative voltage level. In contrast, in TTL systems, the logical one state is at a positive voltage and logical zero is at ground potential.

An advantage of designing with ECL circuitry is that ECL circuits employ differential amplifiers, so you can develop simultaneous complementary outputs without using extra inverters. You can thus reduce package count, power requirements, and timing-differential problems in your design.

Further, all ECL circuits feature open-emitter outputs. If you're using these outputs to drive transmission lines that already provide an output load, you won't need to use internal pull-down resistors, so system power requirements will be further reduced. And, because of the open-emitter design, you can easily tie the outputs of two or more ECL gates together to achieve an OR function without incurring any gate delay. Although some TTL gates (open-collector types) also let you tie the outputs together, all ECL gates give you this capability.

The open-emitter design and complementary-output features of ECL technology give you a great deal of flexibility in logic-system design. Although the power dissipation per gate is lower in TTL devices than in ECL devices, if you were to implement identical logic functions in TTL and ECL, the power/speed ratio of the ECL design might well be better.

Another system-design benefit of ECL is that it doesn't require you to terminate unconnected inputs externally, so it saves pc-board real estate as well as design time and eases automatic testing. To drain off the transistor leakage current, you must pull ECL gate inputs down to V_{EE} through a large-value resistor (50 kΩ for most logic functions). This scheme holds unconnected inputs at logical zero, so you can leave the inputs open. In contrast, Schottky TTL circuits don't allow you to leave unconnected inputs open.

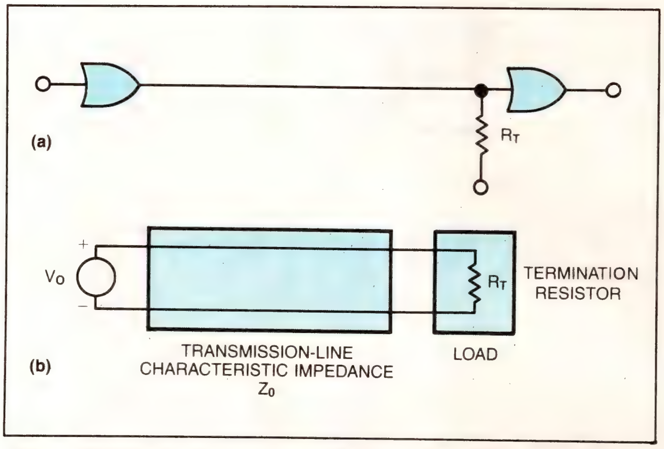


Fig 2—Think of an interconnect between two ECL gates (a) *as a transmission line* ***(b)*** *whose characteristic impedance is Z_0. To minimize ringing in the interconnect, make sure the termination resistance (R_T) matches the line's characteristic impedance (Z_0).*

Moreover, because they exhibit high input impedance and low output impedance, ECL circuits usually have large fan-out and versatile drive capabilities. In addition, the switching-current level is low in ECL devices, so crosstalk between adjacent signal paths is minimal. ECL signals have a typical voltage swing of 850 mV. This voltage swing—lower than that of Schottky devices—shortens system rise and fall times.

Finally, ECL circuits generate minimal power-supply noise. For logic-state transitions, the differential-amplifier design simply switches the current path between two transistors in a mirrored pair. Such a design eliminates current spikes—even during the signal's transition period. Constant power-supply current simplifies power-supply design and reduces system cost.

When you're designing a high-speed logic system, keep in mind that such circuits can often exhibit time delays caused by interconnect-wire inductance; signal distortions caused by transmission-line reflections; crosstalk; and fluctuations in voltage and temperature—any of which can severely limit your system's performance.

You can take a number of steps to minimize these problems. For instance, in high-speed logic systems, each 12-in. length of interconnect wiring introduces a

time delay of approximately 2 nsec—a value approximately equivalent to one gate delay. To avoid possible glitches at the outputs, you can gate the outputs, or you can match input-signal arrival times by using uniform wire lengths or programmable delay lines.

Minimize signal distortions

Signal distortions caused by transmission-line effects are another common problem in high-speed logic systems. In systems that switch at high speeds, the lengths of board interconnects can approach the wavelengths of the signals, causing ringing in the interconnection line. Such ringing signals can cause a false switching indication to an input gate that's directly connected to the other end of the transmission line.

You can solve the ringing problem by using ECL gates. To determine the interaction between wiring and circuitry, treat the interconnections **(Fig 2a)** as transmission lines **(Fig 2b).** You can express this ringing as a function of the line's characteristic impedance and the termination load. Whenever the signal generator changes its output state, the characteristic impedance (Z_0) determines the transient signal on the transmission line, and the termination load (termination resistance R_T, in this case) determines the steady-state signal.

Impedance match eliminates ringing

By selecting the value of R_T to match that of Z_0, you can eliminate ringing in the interconnect lines. When the values of R_T and Z_0 match, you don't have to make any signal adjustments between the transient and steady states. In effect, the system behaves as if the transmission line didn't exist and as if the terminating resistance was connected directly across the generator terminals.

You can use two different techniques to select the value of R_T to match that of Z_0. For instance, in **Fig 3a,** the emitter-follower output transistors drive a 50Ω transmission line. To match R_T to Z_0, you simply terminate the transmission line to −2V through a 50Ω resistor. Another way to accomplish this impedance match is to terminate the transmission line to −5.2V through a Thevenin equivalent load **(Fig 3b).**

In any case, because ECL gates have an open-emitter configuration, you'll need to use pull-down resistors on unloaded lines. Using termination and damping resistors **(Fig 4)** at the outputs of the ECL gates will help reduce ringing on the inputs of subsequent gates. If you connect the pull-down resistor to −5.2V, as in **Fig 4a,** typical values for the resistor (R_P)

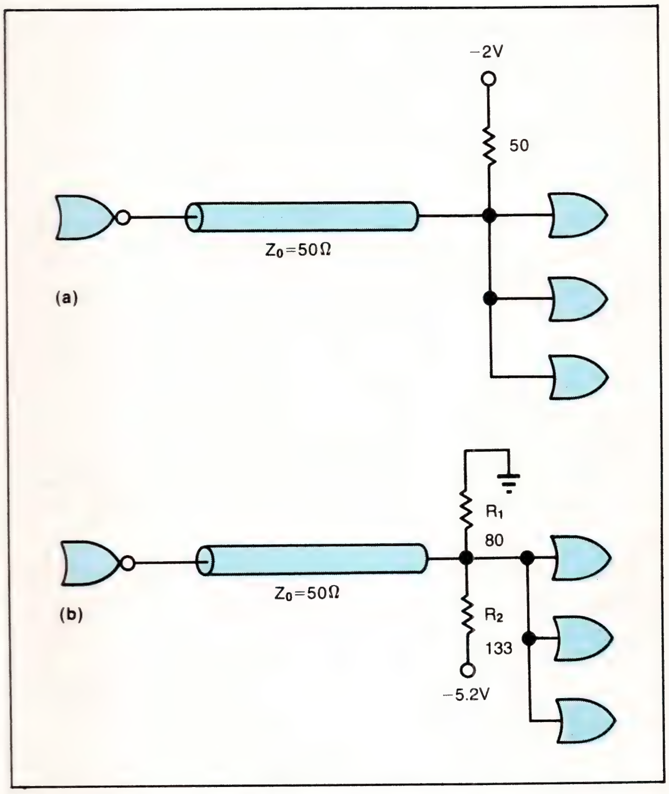


Fig 3—By matching load and transmission-line impedances, *you also reduce unwanted ringing. To effect this impedance match, connect the load resistance to −2V either directly **(a)** or with a Thevenin equivalent termination **(b).***

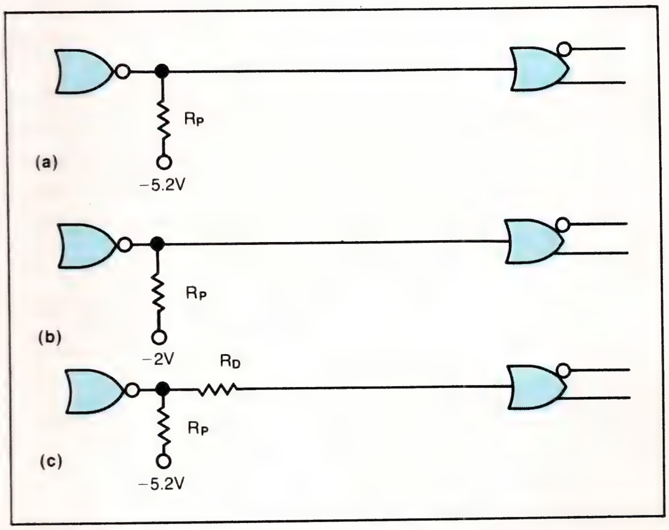


Fig 4—You can reduce unwanted ringing *on ECL-gate inputs by using pull-down and damping resistors. A pull-down resistor connected to −5.2V **(a)** can range from 270 to 2000Ω, depending on the gate's load. To save power, connect the pull-down resistor to −2V **(b).** To drive longer unmatched-impedance interconnections, add a damping resistor **(c).***

An ECL transistor can achieve a switching speed of 750 psec to 1 nsec per gate—roughly two to three times the speed that a Schottky TTL device can offer.

will range from 270Ω to 2 kΩ, depending on load requirements. To save power, connect a 50 to 150Ω resistor (R_P) from the output to −2V **(Fig 4b)**. Further, by using a damping resistor (R_D in **Fig 4c**), you'll be able to use longer unmatched interconnections, although you'll have to sacrifice some switching speed.

Another way to reduce ringing is to use a series-terminated transmission line, which takes advantage of the ringing that occurs at the ends of open lines. Only 50% of the logic swing propagates through these lines. However, an ECL gate's high input impedance approximates the effect of an open line; ringing on an open line doubles the logic swing at the ECL input gate, thereby re-establishing a full logic swing **(Fig 5)**. When you use this series-termination technique, your ECL circuitry generally consumes less power and can usually drive multiple lines.

ECL devices can also minimize crosstalk, another problem typical of systems that switch at high speeds. To reduce the potential for crosstalk in your system, use 10K or 10KH ECL devices, which deliberately slow switching speeds to minimize crosstalk without compromising other performance parameters.

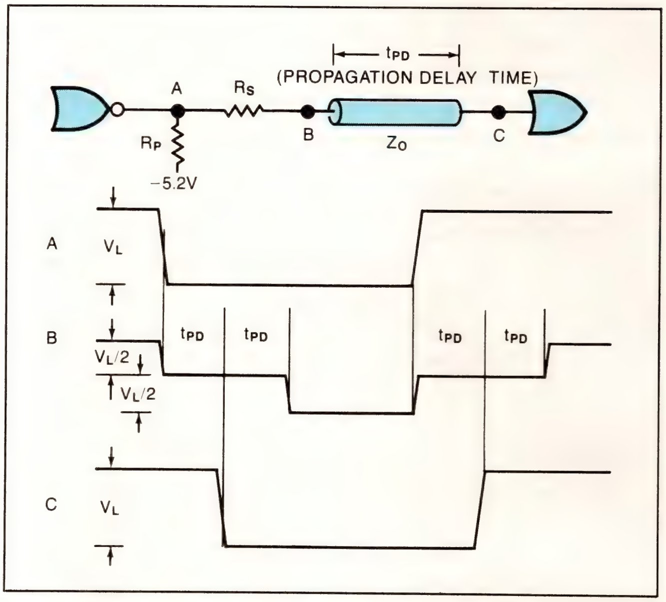


***Fig 5—The series-terminated transmission line** provides another means of reducing ringing. When you use this series-termination technique, your ECL circuitry will consume less power and experience less crosstalk.*

Because variations in voltage and temperature produce fluctuations in threshold and signal levels in your system, you must usually incorporate circuitry that compensates for voltage and temperature changes. In both 10KH and 100K ECL technologies, regulation of the current source and the reference voltages to the balanced-amplifier stage provides voltage compensation. This regulation keeps input-voltage thresholds

10K, 100K, and 10KH ECL technology

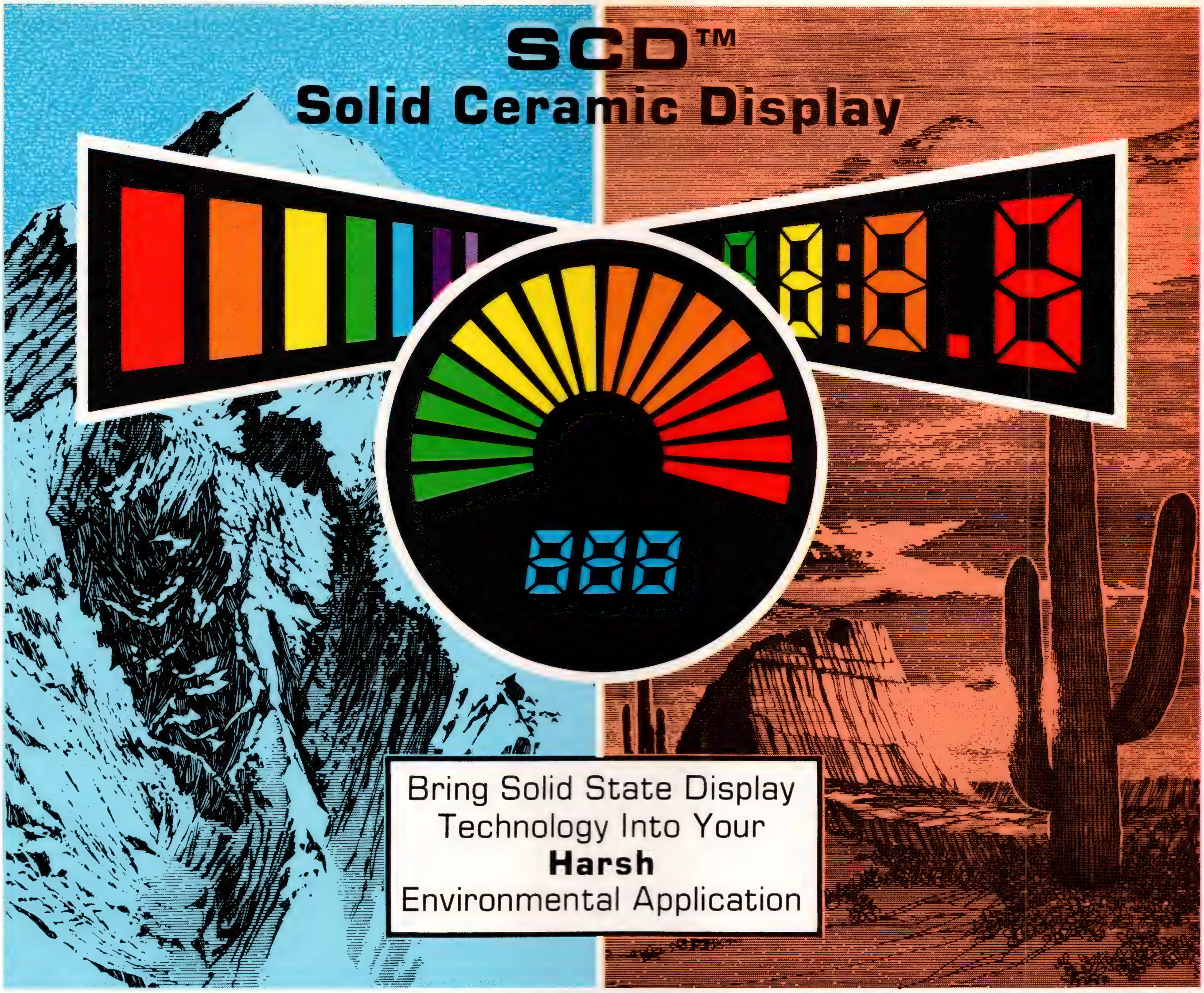
ECL circuitry belongs to three major families: 10K, which was introduced in the early 1970s, and 100K and 10KH, which were both developed in the early 1980s. Improvements in lithographic technology during this time period resulted in 100K and 10KH devices with generally better speed/power characteristics than those of 10K units.

In addition, second-generation ECL circuits (100K and 10KH) have built-in temperature compensation. Devices in the 100K family have compensation circuitry, which counters both voltage and temperature fluctuations. The compensation circuitry in 10KH devices counters voltage fluctuations and simultaneously widens noise margin by 20%. Although their circuit configuration differs from family to family, all ECL devices are compatible; all can coexist on a pc board with little need for special design techniques.

ECL-TECHNOLOGY PERFORMANCE CHARACTERISTICS

PERFORMANCE PARAMETERS	HD10131 (10K)	HD100131 (100K)	MMI10H131 (10KH)
MAXIMUM FREQUENCY (MHz)	125	325	250
EMITTER CURRENT* (mA)	28	50	31
NOISE MARGIN (mV)	125	130	150

ALL DEVICES ARE TYPE-D FLIP-FLOPS.
*TOTAL CURRENT CONSUMED PER FLIP-FLOP



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Because they exhibit high input impedance and low output impedance, ECL circuits usually have large fan-out and versatile drive capabilities.

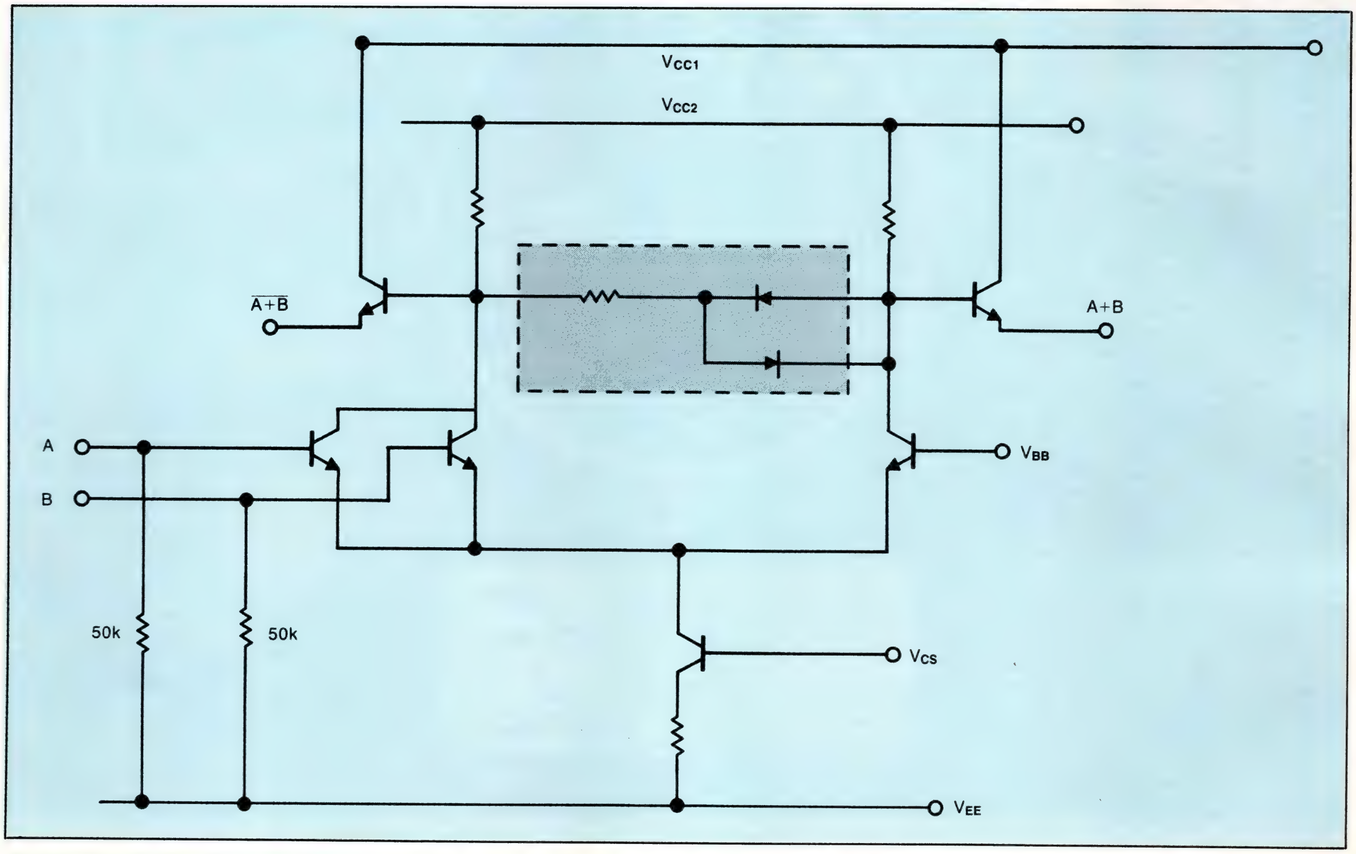

Fig 6—Regulating V_{BB} and V_{CS} *in this ECL circuit eliminates input-threshold sensitivity to temperature and V_{CC} fluctuations. In addition, the diode-resistor network makes the output-voltage levels insensitive to temperature variations.*

constant despite temperature variations and V_{CC} fluctuations. In addition, a simple network between the bases of the output transistors **(Fig 6)** makes the output-voltage levels of 100K ECL circuits insensitive to temperature. Because they have a higher noise margin at the inputs, 10KH ECL devices don't require output-voltage level compensation.

When you use 10KH or 100K ECL devices, you won't require an extended thermal stabilization period during system test. And because the circuits' output swing is not dependent on temperature, thermal gradients across the system aren't a design constraint, so you'll find it easy to design your system's cooling apparatus.

When you're using 10K ECL circuits, however, the temperature gradients are a design constraint; these logic families don't offer temperature compensation. In systems that include uncompensated circuits whose output-voltage levels and input thresholds vary with temperature, it's especially important to minimize temperature gradients between communicating circuits. When driving and receiving circuits are operating at different temperatures, any temperature-induced variations in output-voltage levels and input thresholds will degrade noise-margin figures by about 1 mV/°C of temperature gradient. **EDN**

Author's biography

Kenneth Chan is a senior marketing engineer at the Advanced Logic Div of Monolithic Memories Inc (Santa Clara, CA). His duties include management of an arithmetic product line, market research, and new-product planning for all nonprogrammable products. Ken has BSEE, MSEE, and MBA degrees from Cornell University. He lists fishing, camping, traveling, and outdoor photography among his hobbies.

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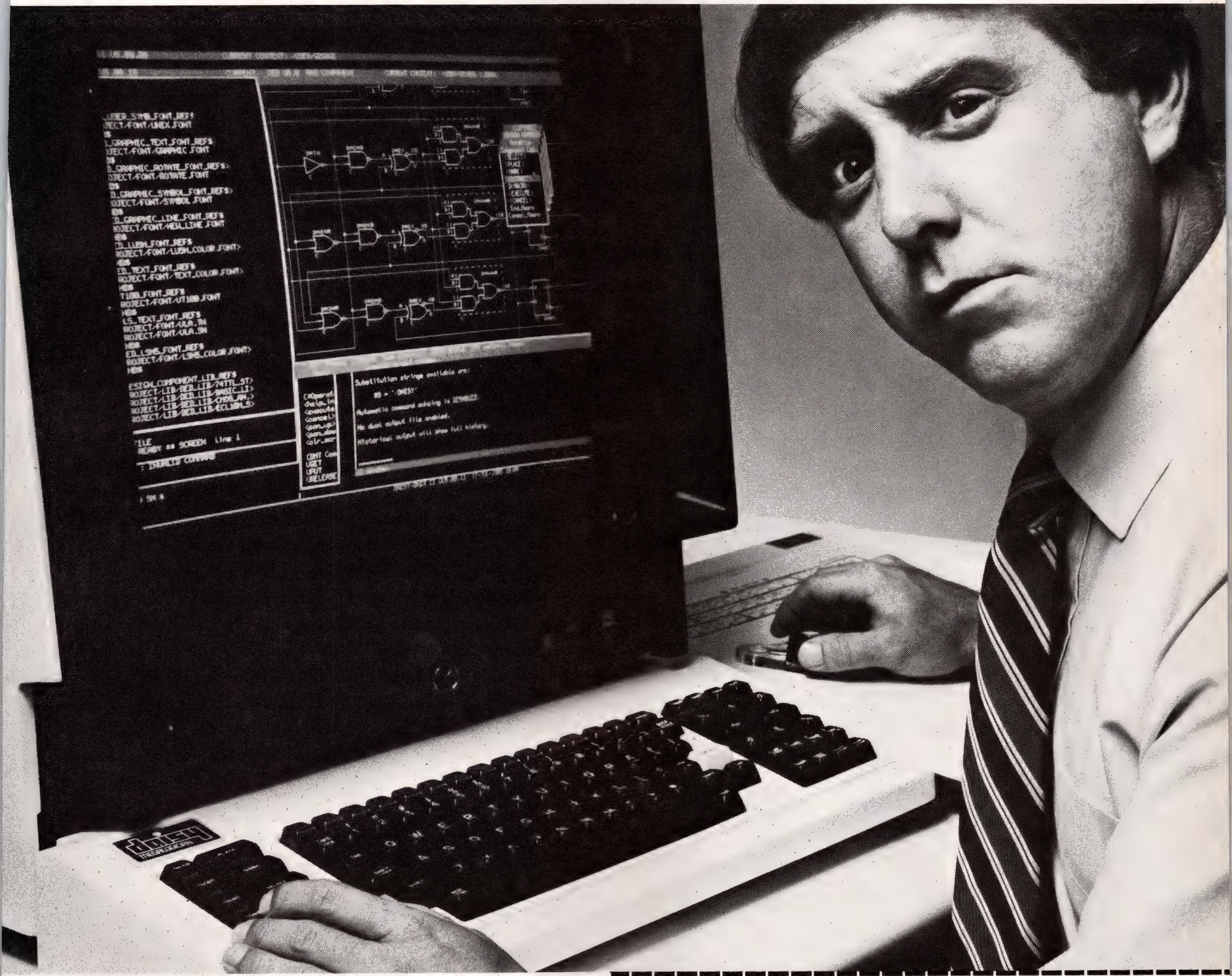

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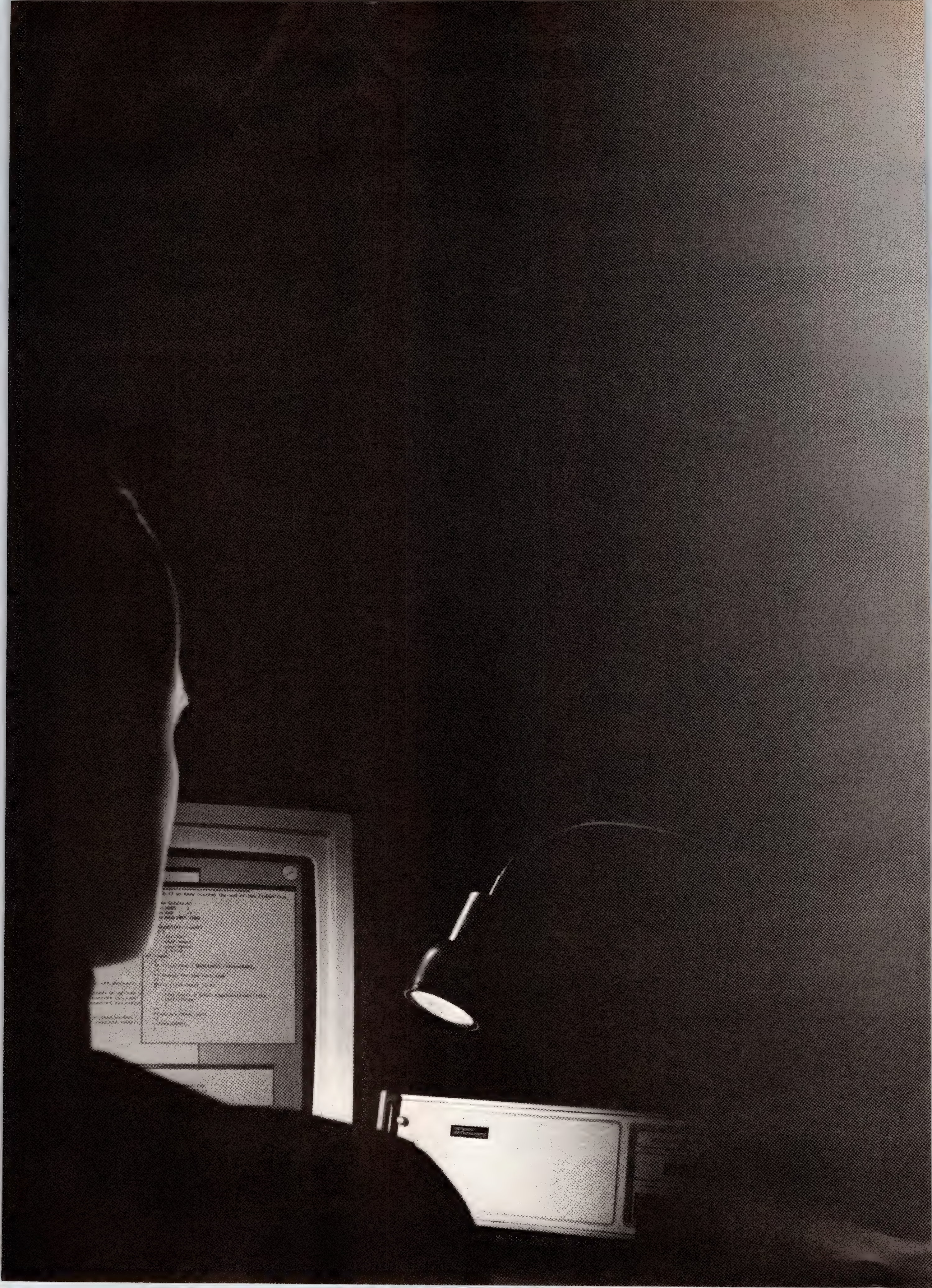

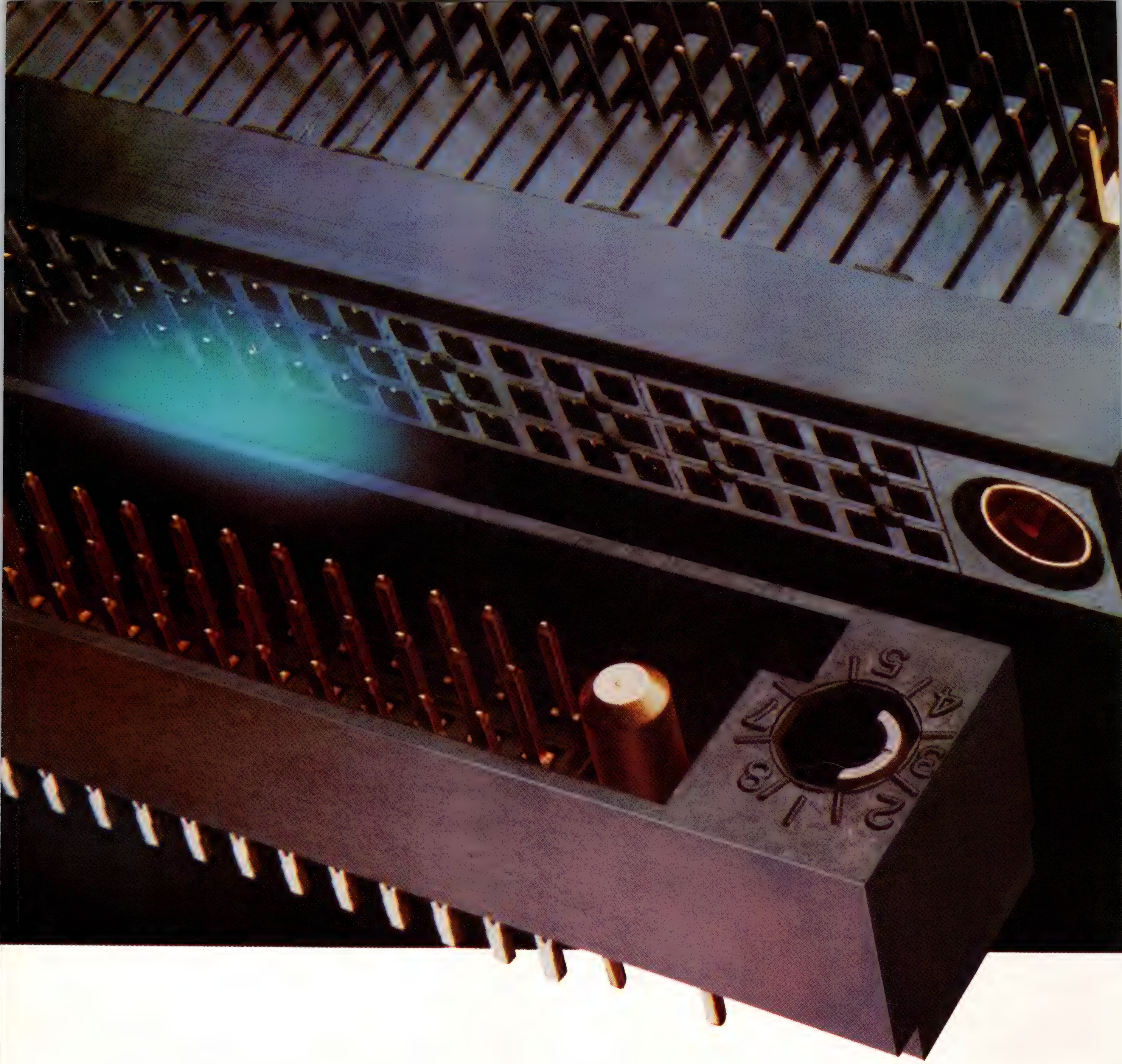

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Single-chip, 2-port RAM controller saves board space

Dual-port RAM chips with built-in control circuitry have prohibitive limitations when considered as solutions to the problem of sharing large amounts of memory between system peripherals. A compact, single-chip, dual-port RAM controller can help processors with different architectures share memory blocks of any size.

Jacques Tellier and David Bell,
Matra-Harris Semiconducteurs

When you design a system that incorporates intelligent peripherals, each with its own μP, you might find that the peripherals need to share fairly large amounts of data with the CPU. The most convenient way of implementing shared memory is to use dual-port RAM, but you'll then need complex control circuitry to ensure that access demands from concurrent, asynchronous processors are served correctly. You can achieve the required level of complexity and still save board space by using a single-chip, dual-port RAM controller.

Dual-port RAM chips with built-in controllers can provide a fast, compact solution to the problem of sharing a small amount of memory. However, current technology limits the capacity of these RAM/controller chips to approximately 2k bytes, and some have only an 8-bit data bus. You can't cascade two or more of these chips to obtain a wider data bus because any slight differences in speed between the chips could produce unpredictable results when two different processors request access simultaneously. To avoid such problems, you would have to access data eight bits at a time, regardless of the bus width.

For a system in which both 8- and 16-bit processors must share memory blocks as large as 64k bytes, you'd like each processor to be able to access as many bits at a time as its native data bus will accommodate. To provide this and other features, however, you'll need a controller that isn't built into the RAM chips. The Matra-Harris HMC6207 dual-port RAM controller provides a compact, low-power means of sharing memory blocks of any size between processors that have different architectures, and of matching the number of memory bits accessed at one time to the data-bus width of the processor making the access request.

The HMC6207 controller chip generates all the signals necessary to interface standard static-RAM chips to two different processor buses, and it generates all the control signals required by 8- and 16-bit processors (**Fig 1**). In addition, the HMC6207 provides the signals required for Multibus control in 80C86/88 systems and performs buffer selection and validation. Fabricated in CMOS, the controller consumes very little power. Internally, the chip has five functional groups of circuitry:

Dual-port RAM/controller chips are available but have limited storage capacity. A separate controller chip is preferable for large shared memories.

arbitration, buffer control, RAM control, acknowledge-signal generation, and Multibus control. The controller has two ports, one for processor A and the other for processor B. There are minor differences between the two ports because the controller was originally designed for use with a Multibus-compatible CPU board based on the 80C86 μP chip.

Controller arbitrates memory requests

To request access to the dual-port RAM, a processor generates one of two request signals: $\overline{\text{A.DRQ}}$ (for the A port) or $\overline{\text{B.DRQ}}$ (for the B port). Either request signal, accompanied by an appropriate read or write signal, causes the request to be stored in the controller in a set of D-type flip-flops that are clocked from an external source. The clock signal may be any signal (usually the system clock of one processor) that satisfies the timing constraints of both processors.

This request-clocking signal will be completely asynchronous with respect to access requests issued by at least one, and perhaps both, of the processors. Therefore, you will not be able to guarantee the setup and hold times of the D-type flip-flops. Under these conditions, cross-coupled TTL or ECL flip-flops would exhibit a tendency toward metastability that would seriously restrict the maximum clock speed. However, the CMOS flip-flops in the HMC6207 have a more stable structure that doesn't use cross-coupling and isn't prone to oscillation or undefined levels.

A priority network (the arbitration section of **Fig 1**) directs the access requests into a second set of D-type flip-flops that control generation of the output signals. If two access requests arrive simultaneously, the controller gives priority to the request from processor A; it will generally service the request from processor B immediately after the memory cycle that services the request from processor A. However, asserting the $\overline{\text{A.LOCK}}$ or $\overline{\text{B.LOCK}}$ signal at the time of the first

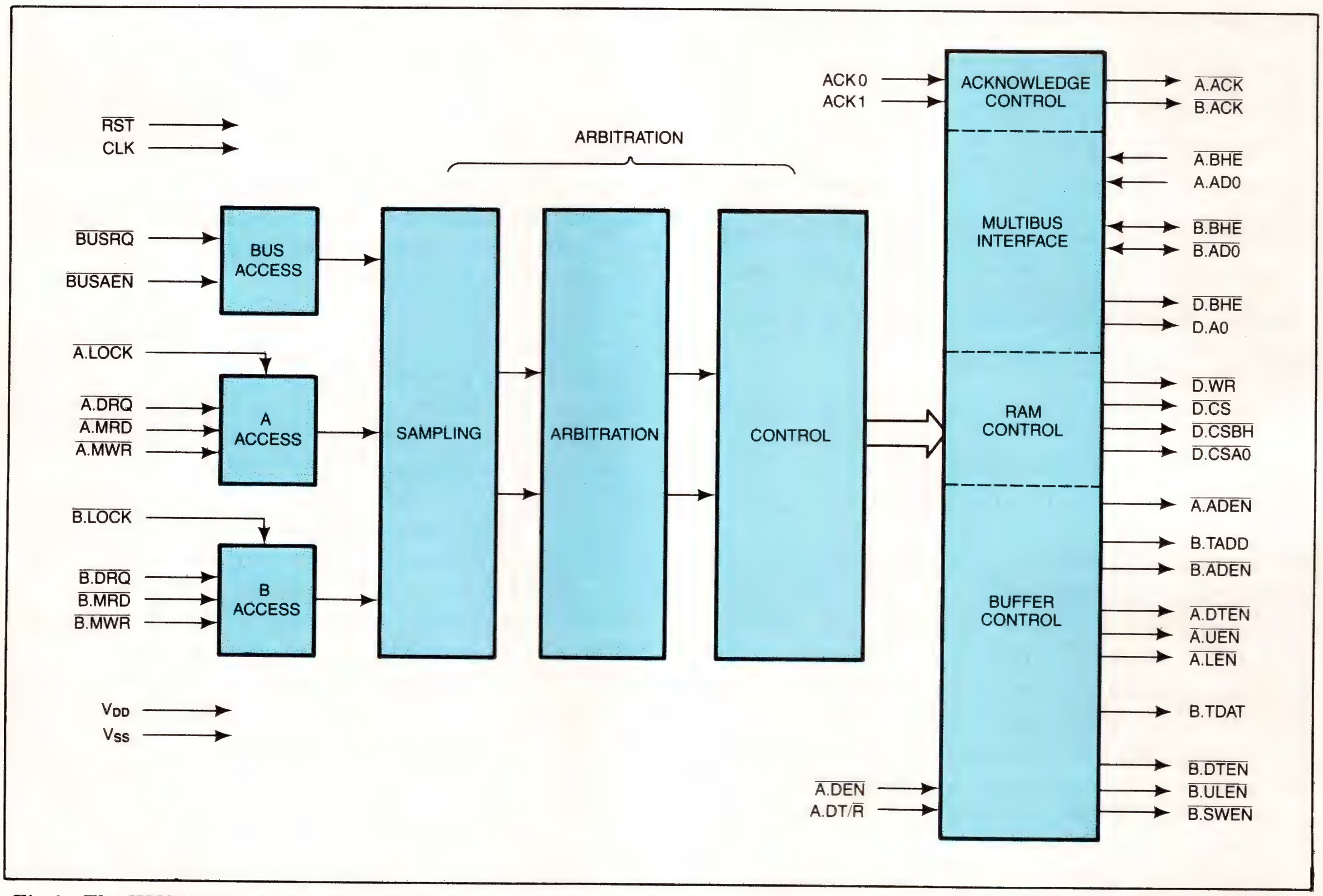

*Fig 1—**The HMC6207 generates all control signals** needed to allow two processors to share a block of static RAM. The processor buses are isolated from each other and from the RAM bus by 3-state buffers.*

access request allows the requesting processor to retain control of the dual-port RAM for as long as the lock signal remains asserted. The controller will deny access requests from the other processor until the lock is removed. The lock operation is useful during loading or updating of data, when accesses by the other processor could produce erroneous results.

The dual-port RAM must have its own address and data buses, isolated from each processor by 3-state, bidirectional buffers. The controller generates all of the signals necessary to control the direction and validation of the buffers.

Further decoding may be necessary

You address individual RAM chips in the dual-port block in the usual manner, using the chip-select signal ($\overline{\mathrm{D.CS}}$). In systems with large amounts of RAM, you may need to perform further decoding on the chip-select signal. You select read or write operations with the write signal ($\overline{\mathrm{D.WR}}$). For reading data, you also assert one of the data-enable signals ($\overline{\mathrm{A.DTEN}}$ or $\overline{\mathrm{B.DTEN}}$).

If you want to organize the dual-port RAM as 16-bit memory, you can select either the low (even) byte with the $\overline{\mathrm{D.CSA0}}$ signal, or the high (odd) byte with the $\overline{\mathrm{D.CSBH}}$ signal. The lower-byte enable ($\overline{\mathrm{A.LEN}}$) and upper-byte enable ($\overline{\mathrm{A.UEN}}$) signals activate a separate data buffer for each half of the memory word, so that by asserting the proper signals you can use 16-bit memory with one 16-bit and one 8-bit processor, or with two 16-bit processors, or even with two 8-bit processors.

When an access request is being serviced, the con-

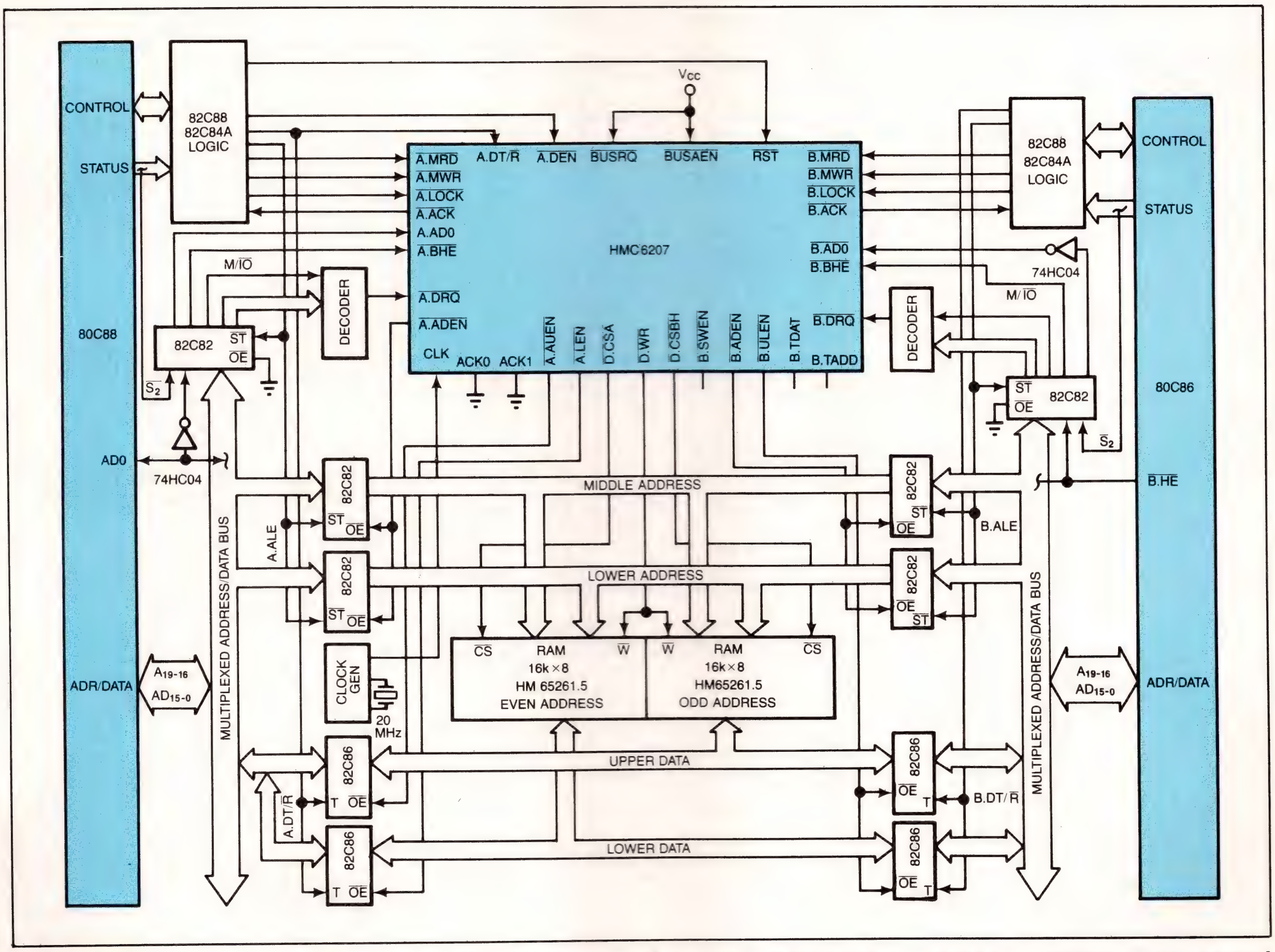

Fig 2—An 8-bit processor can share memory with a 16-bit processor by using the HMC6207 dual-port RAM controller and some external logic.

Many intelligent peripherals must share memory with the host processor to maintain high data-transfer rates.

troller generates an acknowledge signal ($\overline{\text{A.ACK}}$ or $\overline{\text{B.ACK}}$) to inform the requesting processor that data is ready. Normally, such signals appear on the control bus at the same time that the controller generates the chip-select signal. This synchronicity allows an access time of approximately 100 nsec for the RAM.

If, however, your system requires longer access times—you're using slow RAM, for example—applying an appropriate code (01, 10, or 11) to the ACK0 and ACK1 pins of the controller lets you delay both acknowledge signals (for all accesses) by one, two, or three clock states. The extra access time may be as little as 50 nsec or as much as 100 nsec, depending on the controller clock rate.

As noted, the controller interfaces to the Multibus, which allows both 8-bit and 16-bit data transfers. You select a Multibus access by asserting the bus-request ($\overline{\text{BUSRQ}}$) and bus-address-enable ($\overline{\text{BUSAEN}}$) signals. The controller then passes the address generated by the processor to the Multibus via the dual-port RAM address bus. At the same time, the controller places the proper byte-select signals on the Multibus.

All 8-bit transfers take place on data lines $D_{0\text{-}7}$, the even byte. If you want to read an odd byte, you must transfer the byte from RAM data lines $D_{8\text{-}15}$ to Multibus data lines $D_{0\text{-}7}$. For a write operation, you transfer the odd byte from Multibus lines $D_{0\text{-}7}$ to RAM data lines $D_{8\text{-}15}$. The usual way of doing the swap is to transfer the byte through an extra buffer called the swap buffer. The HMC6207 decodes $\overline{\text{B.AD0}}$ and $\overline{\text{B.BHE}}$ and generates either the upper-and-lower-byte enable signal ($\overline{\text{B.ULEN}}$) for a 16-bit transfer or the swap-enable

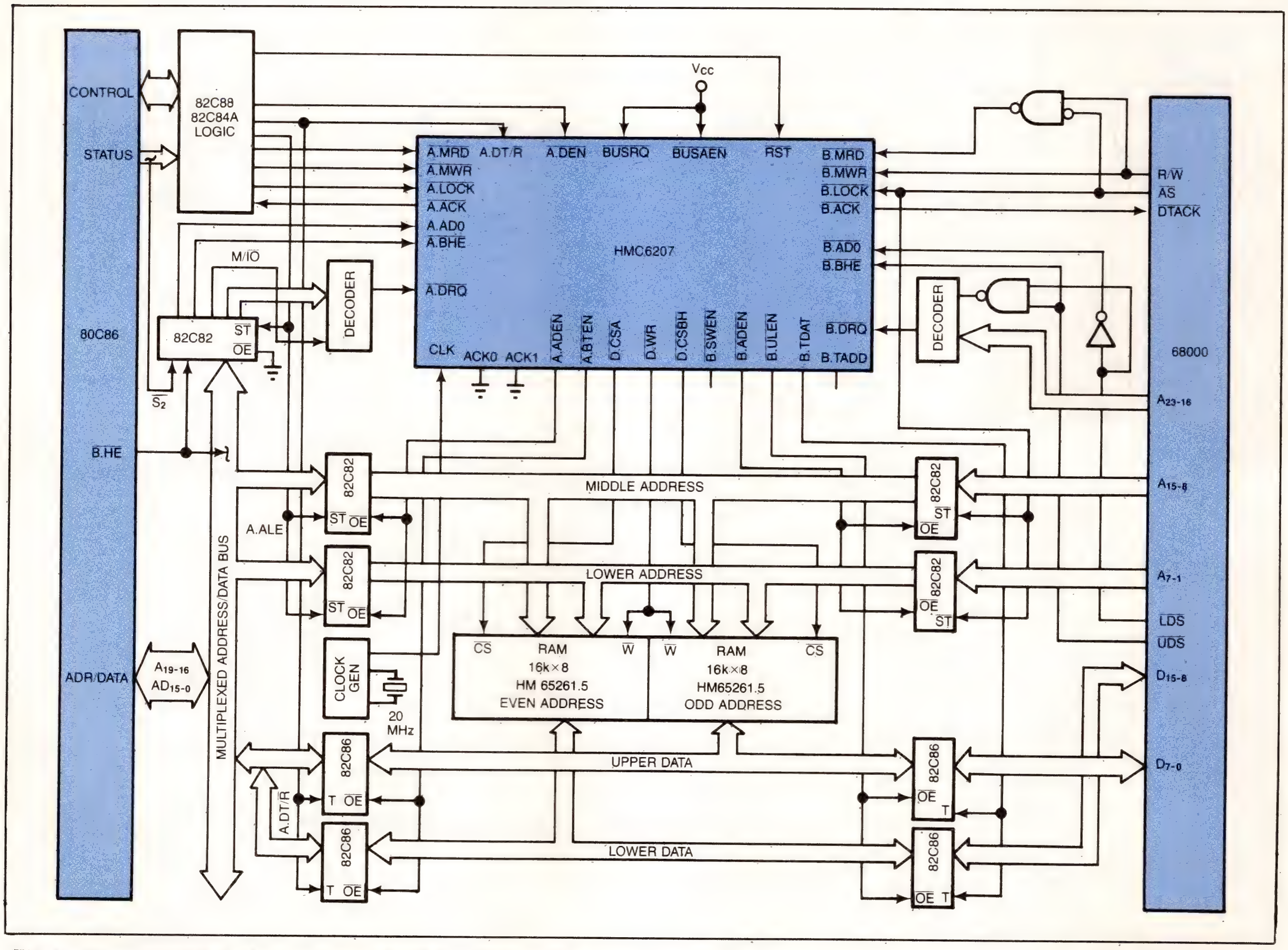

Fig 3—Processors that share memory don't have to be of the same family. You can connect an Intel processor to one port of the RAM controller and a Motorola processor (or a Multibus multimaster system) to the other port.

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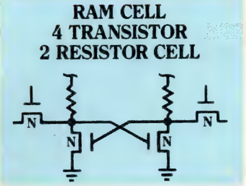

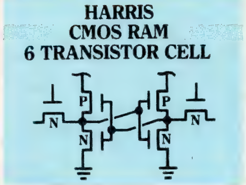

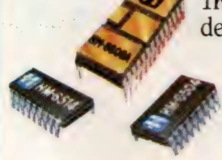

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CIRCLE NO 86

TABLE 1—PROCESSOR A ACCESS TO DUAL-PORT RAM

$\overline{\text{A.BHE}}$	$\overline{\text{A.AD0}}$	ACCESS TYPE
0	0	16-BIT ACCESS TO RAM. SIGNALS $\overline{\text{D.CSBH}}$ AND $\overline{\text{D.CSA0}}$ ARE ACTIVE.
1	0	8-BIT ACCESS TO EVEN BYTE. DATA IS TRANSFERRED ON DATA LINES D_{0-7}. SIGNALS $\overline{\text{D.CSA0}}$ AND $\overline{\text{A.LEN}}$ ARE ACTIVE.
0	1	8-BIT ACCESS TO ODD BYTE. DATA IS TRANSFERRED ON DATA LINES D_{8-15}. SIGNALS $\overline{\text{D.CSBH}}$ AND $\overline{\text{A.UEN}}$ ARE ACTIVE.
1	1	ILLEGAL. THE PROCESSOR MUST NOT MAKE AN ACCESS WITH THE SIGNALS IN THIS STATE.

signal ($\overline{\text{B.SWEN}}$) for an odd-byte transfer. **Tables 1** and **2** show the various kinds of transfer that are legal and the signals that you must assert to select a particular type of transfer.

Fig 2 shows how an 8-bit 80C88 processor can share a 16k-byte block of memory with a 16-bit 80C86 processor. The shared memory is 16 bits wide for the benefit of the 80C86. Access to the shared memory is through port A for the 80C88 and through port B for the 80C86. In the configuration shown, the control signals generated by each processor determine the direction of the buffers, and the 80C88 cannot access the local bus of the 80C86.

If it becomes necessary for the 80C88 to access devices attached to the 80C86 local bus, you'll have to use the Hold and HLDA signals (used for minimum-mode DMA) as follows. First, arrange it so that, when the 80C88 decodes an address that refers to a device on the 80C86 local bus, the $\overline{\text{BUSRQ}}$ signal will be applied to the 80C86 Hold input via a synchronization flip-flop. Then connect the $\overline{\text{HLDA}}$ signal, which releases the 80C86 bus, to the $\overline{\text{BUSAEN}}$ input of the controller; the 80C88 now has access to the 80C86 local bus. You'll need to implement some additional logic to pass the acknowledge signal to the 80C88. In particular, this logic should invert the AD0 signal from the 80C86 before address decoding takes place.

Although the HMC6207 RAM controller interfaces primarily with processors of the Intel family, it's flexible enough to accommodate processors that have quite a different architecture, such as members of the Motorola 68000 family. **Fig 3** shows how you can share memory between 80C86 and 68000 processors. The 68000 generates and requires signals that are very similar to those of the 80C86. There are, however, some discrepancies, and connecting the 68000 to port B (originally designed as the Multibus port) will make it easier to correct them.

The 68000 uses the upper data strobe (UDS) and lower data strobe (LDS) to indicate access type. These signals correspond directly to the $\overline{\text{BHE}}$ and AD0 signals of the 80C86, but you must invert the LDS signal.

TABLE 2—PROCESSOR B ACCESS TO DUAL-PORT RAM

$\overline{\text{B.BHE}}$	$\overline{\text{B.AD0}}$	ACCESS TYPE
0	1	16-BIT ACCESS TO RAM. SIGNALS $\overline{\text{D.CSBH}}$, $\overline{\text{D.CSA0}}$, AND $\overline{\text{B.ULEN}}$ ARE ACTIVE.
1	1	8-BIT ACCESS TO EVEN BYTE. DATA IS TRANSFERRED ON DATA LINES D_{0-7}. SIGNALS $\overline{\text{D.CSA0}}$ AND $\overline{\text{B.ULEN}}$ ARE ACTIVE.
1	0	8-BIT ACCESS TO ODD BYTE. DATA IS TRANSFERRED ON DATA LINES D_{8-15}. SIGNALS $\overline{\text{D.CSBH}}$ AND $\overline{\text{B.SWEN}}$ ARE ACTIVE.
0	0	8-BIT ACCESS TO ODD BYTE. DATA IS TRANSFERRED ON DATA LINES D_{8-15}. SIGNALS $\overline{\text{D.CSBH}}$ AND $\overline{\text{B.SWEN}}$ ARE ACTIVE.

To ensure that the controller can generate all the buffer signals necessary for a data transfer, combine the read/write ($R/\overline{W}$) and address-strobe ($\overline{\text{AS}}$) signals to produce the $\overline{\text{B.MRD}}$ and $\overline{\text{B.MWR}}$ signals. You should also connect the address strobe to the $\overline{\text{B.LOCK}}$ input of the controller to ensure that the 68000 has control of the RAM during test-and-set instructions. Finally, connect the controller's $\overline{\text{B.ACK}}$ signal directly to the $\overline{\text{DTACK}}$ input of the 68000. **EDN**

Authors' biographies

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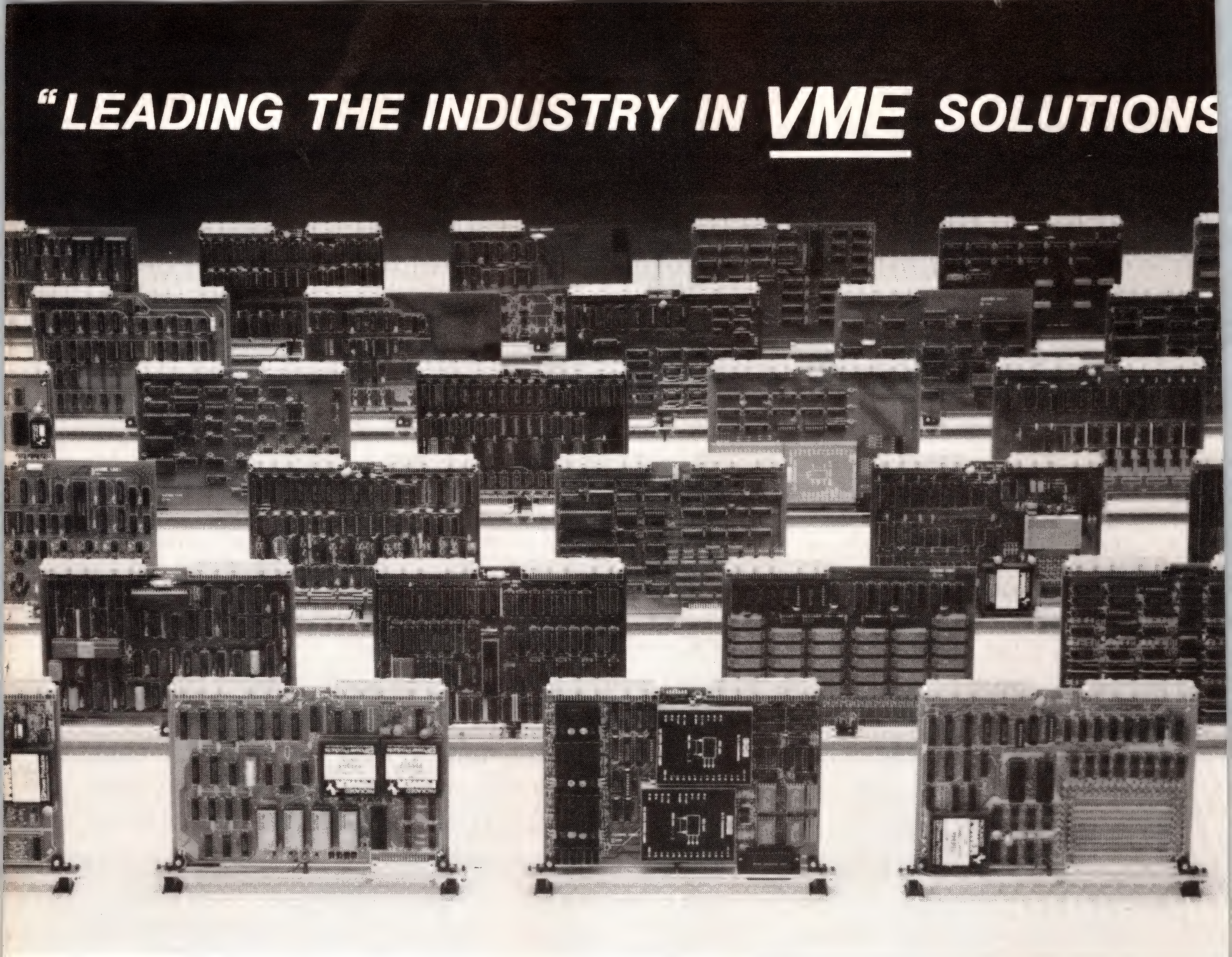

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CIRCLE NO 89

Software links math chip to 68000-family μPs

Emulating the MC68020 μP's special coprocessor instructions gives you two ways to link an MC68881 math chip and 16-bit 68000-family CPUs. You use macros to insert coded routines in your program, or you use a trap routine that detects and emulates special math op codes.

Sarah Harris and Tom Johnson, *Motorola Inc*

Although it's specifically designed for use as a coprocessor with the 32-bit MC68020 μP, the MC68881 floating-point math chip also operates with 16-bit 68000-family μPs. If you interface the 68881 chip to a computer as a peripheral device rather than as a coprocessor, you get to choose between two types of control software for the chip: in-line code such as macros or trap and emulation routines. You can adapt the macros to many μPs, but the trap technique is specific to the 68000 family, which includes the MC68000, MC68008, MC68010, and MC68012 chips.

When you use a 68881 math chip as a coprocessor in a 68020-based computer system, the interface circuit places the math chip's registers in the CPU's address space. The 68020 μP chip selects the CPU address space by setting its function-code output lines FC_0-FC_2 to 111. The 16-bit 68000 μP chip, however, doesn't allocate any CPU address space; instead, it identifies an interrupt-acknowledge cycle with the equivalent function code. Therefore, to properly control a 68881 chip in a 68000-based computer, you must design the interface circuit to control the math chip as a peripheral device in the computer's data-address block.

When the 68881 math chip is available to your computer as a peripheral, you can write the control software in two ways. The first approach involves writing macros or in-line code that controls the math chip. You use standard 68000 op codes that treat the math chip as a peripheral device, transferring instructions and data to it and receiving flags and data from it. Each macro or section of in-line code acts as a driver routine that simulates one of the 68020's special coprocessor op codes. If your software-development tools don't support macros, you can write subroutines instead.

Trap routines decode op codes

The second approach lets you include the 68020's coprocessor op codes in your program along with the usual 68000 op codes. Although the 68000 family's 16-bit CPUs don't execute the coprocessor op codes, they do detect or trap them, forcing the CPUs into an exception state. While it's in the exception state, a 68000 CPU transfers control to a routine that decodes the coprocessor op code and emulates it with a series of 68000 instructions that control the 68881 math chip.

Each coprocessor op code contains bits that identify a

Macro routines let you insert 68881 control operations into your programs.

general, branch, conditional, save, or restore operation. The op code also contains three identification bits that let the computer select one coprocessor from as many as eight **(Fig 1)**. After each coprocessor op code you'll include as many as seven words that contain a coprocessor command, data, address, and extension information, depending on the type of op code. Keep in mind that the coprocessor op code simply signals the CPU that coprocessor information follows. The command and data words that follow the op code control the coprocessor.

Because the four most significant bits in each coprocessor op code are set to a logic one, or hexadecimal F, programmers call the coprocessor instruction trap the F-line trap. Although using the F-line trap technique means you'll have to write control routines that simulate the coprocessor instructions, there's an advantage to using the trap technique if you plan to transfer your programs to a 68020 CPU. Because the 68020 executes the special coprocessor instructions without forcing the CPU into an exception state, moving up to a 68020-based computer requires no software changes. You might, however, want to remove the coprocessor instruction-emulation subroutines from your 68000 program to save memory space. A disadvantage of using the F-line trap technique in 68000 systems is that the exception processing takes extra time (the CPU must perform stack and vector operations), and your subroutine must interpret the 68881 instruction, data, and address information that follows each coprocessor op code.

Techniques trade memory for time

The trade-off between the macro and instruction-emulation techniques involves program-execution time vs program length. Each time you put a math-coprocessor macro in your program, you increase the program's length, but the program still operates quickly. On the other hand, by using emulation routines you save program space, because you need only one routine per function. Emulation routines, however, require CPU time to perform internal operations and to decode the 68881's instructions. So if processing speed is of prime importance, use macros.

By using macros, software-development systems will quickly insert the math-chip control steps into your program as you need them. If your assembler supports parameter manipulation within macros, use the assembler to parse the 68881 chip's math instructions and to determine the proper addressing mode for them. Similarly, if you can include conditional-assembly directives within the macros, the assembler will decode bit fields in the math instructions to determine what actions you want the final program to perform. Because the assembler does the parsing and decoding as part of the program-development process (ie, at assembly time), the resulting program runs efficiently and quickly.

How you define the control macros for the 68881 math chip depends on your application. Under ideal conditions, you'd program a macro for each 68881 math operation using standard 68881 instruction mnemonics as the macro name. When you provide separate math-operation macros, the software is source-code compatible with a 68020 μP chip; you simply reassemble the code with a 68020 assembler. However, you'll need a lengthy library of macros for all combinations of 68881 math operations, data types, and addressing modes.

Instruction groups save programming time

With the exception of the Save and Restore instructions, you can put similar instructions in groups and write generalized macros for each group. For example, all of the instructions that transfer data from memory into the 68881 chip operate in the same way. By grouping the instructions, you can write general macros that control each type of memory-to-68881 transfer (these macros are known as "move-in" macros). Let the assembler decode the individual math operations and modify the main sequence of instructions within the macro accordingly. Differences within a group of instructions occur in the math operation to be done (addition, subtraction, etc), the data's type (precision and format), and the addressing mode. Although a smaller number of generalized macros simplifies your programming task, you must still give your macros the same information or parameters you'd find in the coprocessor instructions they replace.

To pass parameters to a move-in macro, use the following general format:

MACRONAME FUNCTION, SOURCE, DESTINATION

MACRONAME specifies the method of data transfer and the data type, while FUNCTION tells the macro what type of general operation you want to simulate **(Table 1)**. SOURCE and DESTINATION are memory or register pointers. The seven general move-in macros differ only in the precision of the information they transfer. The sample macro of **Listing 1** (pg 184) serves

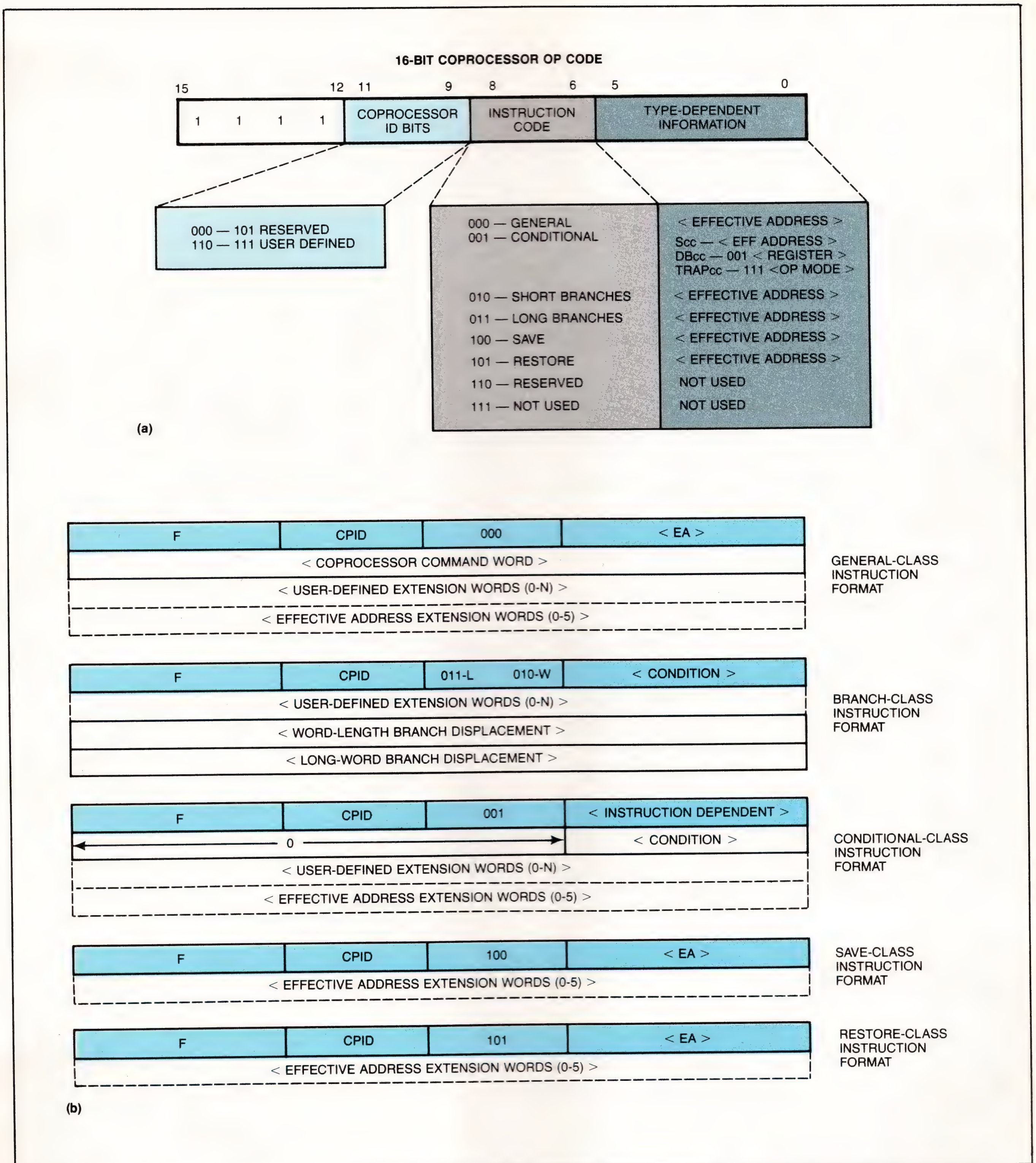


***Fig 1—Coprocessor op-code formats include** an F-line op code that identifies the coprocessor device and the type of operation **(a)**. As many as seven words follow the op code **(b)**, providing a coprocessor command, data, address, or other information.*

The F-line traps provide for upward compatibility with 68020-based computers.

TABLE 1—INFORMATION AND CODES FOR THE MEMREGx MACROS

FUNCTION DATA

MNEMONIC	HEX	FUNCTION	MNEMONIC	HEX	FUNCTION
FMOVE	$00	MOVE	FCOSH	$19	HYPERBOLIC COSIN
FINT	$01	INTEGER PART	FNEG	$1A	NEGATE
FSINH	$02	HYBERBOLIC SIN	FACOS	$1C	ARC COSIN
FSQRT	$04	SQUARE ROOT	FCOS	$1D	COSIN
FLOGNP1	$06	LOG BASE (N + 1)	FGETEXP	$1E	GET EXPONENT PART
FETOXM1	$08	(e**X) – 1)	FGETMAN	$1F	GET MANTISSA PART
FTANH	$09	HYPERBOLIC TAN	FDIV	$20	DIVIDE
FATAN	$0A	ARC TAN	FMOD	$21	MODULO REMAINDER
FASIN	$0C	ARC SIN	FADD	$22	ADD
FATANH	$0D	HYPERBOLIC ARC TAN	FMUL	$23	MULTIPLY
FSIN	$0E	SIN	FSGLDIV	$24	SINGLE-PRECISION DIVIDE
FTAN	$0F	TAN	FREM	$25	IEEE REMAINDER
FETOX	$10	e**X	FSCALE	$26	SCALE EXPONENT
FTWOTOX	$11	2**X	FSGLMUL	$27	SINGLE-PRECISION MULTIPLY
FTENTOX	$12	10**X	FSUB	$28	SUBTRACT
FLOGN	$14	LOG BASE N	FCMP	$30	COMPARE
FLOG10	$15	LOG BASE 10	FTST	$38	TEST OPERAND
FLOG2	$16	LOG BASE 2	FSINCOS	$3A	SIMULTANEOUS SIN AND COS
FABS	$18	ABSOLUTE VALUE			

REGISTER DATA

HEX OFFSET	MNEMONIC	REGISTER NAME
$00	FP0	FLOATING-POINT DATA REGISTER 0
$01	FP1	FLOATING-POINT DATA REGISTER 1
$02	FP2	FLOATING-POINT DATA REGISTER 2
$03	FP3	FLOATING-POINT DATA REGISTER 3
$04	FP4	FLOATING-POINT DATA REGISTER 4
$05	FP5	FLOATING-POINT DATA REGISTER 5
$06	FP6	FLOATING-POINT DATA REGISTER 6
$07	FP7	FLOATING-POINT DATA REGISTER 7
$00	RESPONSE	RESPONSE-INTERFACE REGISTER
$0A	COMMAND	COMMAND-INTERFACE REGISTER
$10	OPER	OPERAND-INTERFACE REGISTER
$838000*	MC68881	BASE ADDRESS OF MC68881 IN DATA SPACE

*THIS VALUE IS SELECTED BY THE USER BASED ON SYSTEM CONFIGURATION.

DATA TYPES

DESIGNATION	DATA TYPE
B	BYTE-INTEGER
W	WORD-INTEGER
L	LONG WORD-INTEGER
S	SINGLE-PRECISION FLOATING POINT
D	DOUBLE-PRECISION FLOATING POINT
X	EXTENDED-PRECISION FLOATING POINT
P	PACKED BCD FLOATING POINT*

*BCD = BINARY-CODED DECIMAL.

as a prototype to use when you develop your own control software.

All move-in macros operate in the following sequence: Write the instruction or data into the proper 68881 register; test the 68881 for a response; respond to a 68881 request; and release the processor for other tasks. During its sequence of operations, the 68881 chip puts information in its response register, forms a primitive instruction from that information, and passes that instruction to the CPU. The response register's most significant bit represents a come-again (CA) flag that tightly couples the 68881 coprocessor to the main CPU in a 68020-based computer.

In computer systems that use the 68881 chip as a peripheral, the CPU treats the CA bit as a busy/ready flag that indicates the status of the 68881 chip. If the CA bit is set, the computer executes the primitive command (if any) in the 68881's response register and then tests the CA bit again. When the CA bit is set and the response register doesn't contain a specific service request, the computer continues to test the CA bit in a null-come-again loop:

```
\@NULREL TST.B MC68881+RESPONSE ;TEST REGISTER
         BMI.S \@NULREL         ;BRANCH ON MINUS
```

After it completes a task, the 68881 chip resets the CA bit, releases the computer from the loop, and lets it go to the next program step. In addition to the CA bit, the response register contains either requests for CPU services or information that alerts the CPU to error conditions in the 68881 chip.

Flag bits detect errors

Because the 68881 implements IEEE Standard 754 math operations, the chip includes many error or exception flags that detect such conditions as overflow and floating-point divide-by-0. The 68881 lets you selectively enable or disable individual exception bits so your software monitors only the ones you choose. The chip's default condition disables all of the exception bits, which eliminates the need to test for their presence and process them in your software. Processing errors can still occur, however; you just won't know they took place. To keep the macro examples simple, the error- or exception-processing steps aren't included. Begin software development at a low level and increase its complexity later. Leave the exception bits disabled until you develop and test the main macros.

If you disable the 68881's exception and error flags, the only response-register commands the CPU gets are null-come-again or evaluate-effective-address-and-transfer-data commands. The latter type of command directs the computer to transfer information to or from the 68881 chip. After you're familiar with the coprocessor's op codes and instructions, you can start to plan the flow of your macro routines.

Start with sample macro routines

The sample MEMREGW macro **(Listing 1)** operates on a word-length value (16 bits) and illustrates how a typical macro routine operates **(Fig 2)**. The macroroutine call within your main program takes the form

MEMREGW FUNCTION, EA, FPN

Within the macro routine, the computer equates each function code (FUNCTION) and internal 68881 register number (FPN) with a specific bit pattern. The assembler combines these bit patterns with the effective-address (EA) value to formulate the proper 68000

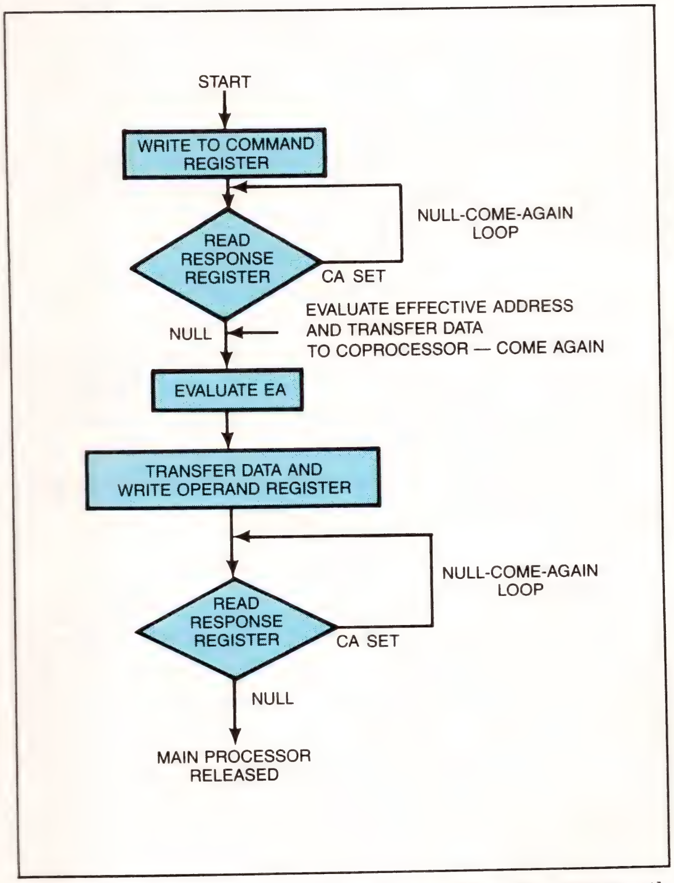


***Fig 2—The move-in macros transfer information** to the 68881 math chip and monitor the come-again flag bit until it releases the computer.*

Prototype macro and trap routines provide examples you can adapt to your computer.

instructions that control the 68881 chip.

The assembler accepts the parameters from the macro-calling line in your program in the order you list them. Within a macro routine, you note the first parameter as ¢1, the second parameter as ¢2, and so on. For example, line 69 in the macro listing contains the statement

MOVE.W
#$5000+(¢3<<7)+¢1,MC68881+COMMAND

which combines the third parameter (FPN), the first parameter (FUNCTION), and 5000_{16} to form a 68881 command word of the form F<OP>.W <EA>,FPN **(Fig 2).** The assembler directive ¢3<<7 shifts the floating-point register's address left by seven bits to align it properly in the 16-bit instruction. The MC68881+COMMAND operation sets up the absolute address for the 68881's command register. In the MOVE.W command, the 68881's base address is set to 838000_{16}, while the command register is preset in the chip at address $0A_{16}$. You can assign your 68881 chip a different address, but you can't change the internal 68881 register-address assignments.

After combining the function and register information, the MEMREGW macro uses the second parameter (EA) in the command at line 73:

MOVE.W ¢2,MC68881+OPER

The MOVE.W command assembles an instruction that moves a data word from the effective address into the 68881's internal operand register. Again the assembler combines the 68881's base address with the operand register's address to generate the absolute memory address for the peripheral 68881 chip.

Conditional assembly for some operations

Because the assembler uses a comma to separate parameters, you can't pass the indexed-register-indirect-with-offset parameter (d(An,Rn) or d(Pc,Rn)) directly to the macro. If you try to do so, the assembler finds the comma between An (or Pc) and Rn and attempts to split the information into two parameters. To get the d(An,Rn) information to the macro, the software takes an indirect approach by using a conditional command in the macro routine and passing a fourth parameter to the macro. The IFC '¢4',″ command at line 68 in the MEMREGW macro lets the computer determine how to assemble the program depending on whether or not you supply the fourth parameter. When you supply the fourth parameter, the macro's instructions between lines 77 and 85 combine parameters 2 and 3 to reconstruct the effective address. The macro routine uses the command at line 82 to insert the comma between the parameters for proper assembly of the program.

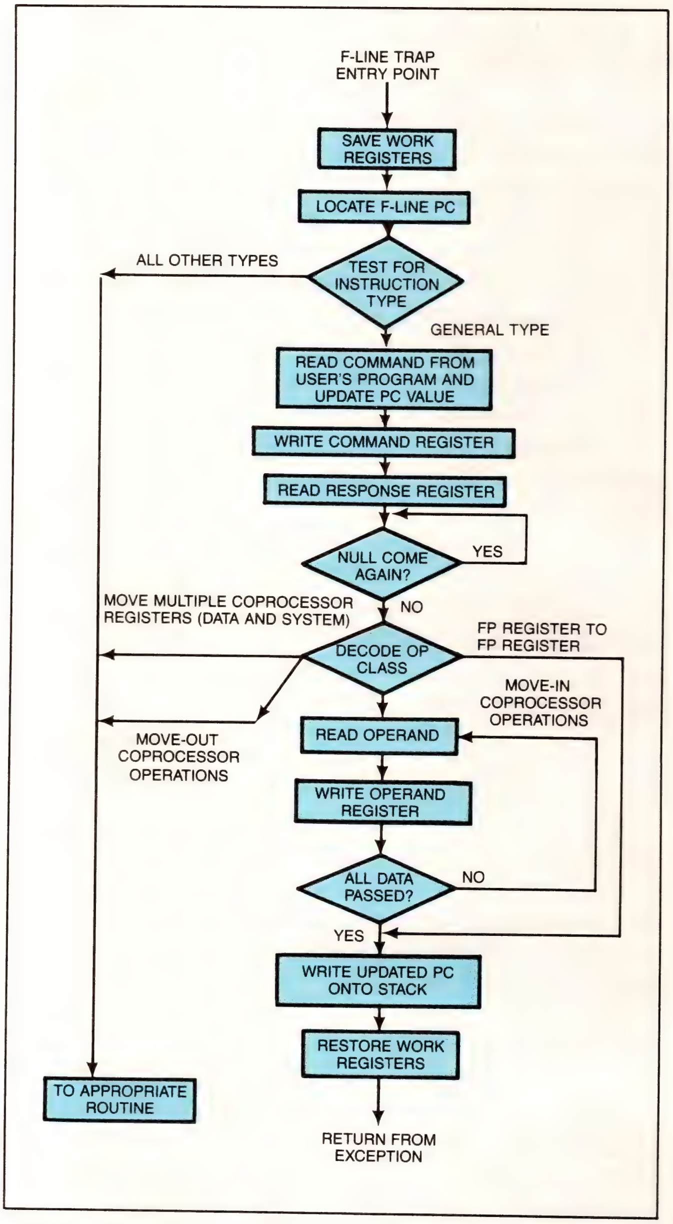


Fig 3—The F-line trap routine requires *extra instructions to locate the coprocessor op code, decode it, and perform the control steps to emulate it. You'll also need to add routines if you want to be able to emulate 68881-to-memory (move-out) and multiple-register instructions.*

Although the 68020 μP chip provides instructions that directly handle packed-BCD (P), double-precision (D), and extended-precision (X) data types—all of which require more than 32 bits—the 68000 doesn't offer you these instructions. Upon detecting one of these three data types, have the macro assemble the necessary instructions that transfer the multiple words of data to the 68881 chip.

Macros provide 68020 upgrade path

When you transfer programs containing math macro routines to a 68020-based μC system, you must change the macros. For example, the following macro assembles a floating-point byte move-in routine:

```
MEMREGB        MACRO
               \1.B \2, \3
               ENDM
```

By providing an FADD code for the first parameter, you tell the assembler you want an addition operation to take place in the 68881 chip. The .B notation indicates a byte operation. The second and third parameters represent the effective-address and 68881 destination-register information. For assembly in a 68020 program, the macro call remains the same, but the internal macro program steps no longer generate long in-line programs. Instead, the macro call

```
MEMREGB     FADD,D0,FP0
```

generates the proper coprocessor math instruction:

```
FADD.B      D0,FP0
```

Although the macro approach provides software compatibility when you transfer your math programs from a 68000- to a 68020-based computer, it doesn't provide a perfect solution. Because the 68000 μP treats the 68881 as a peripheral and the 68020 μP treats it as a coprocessor, you'll have to modify the 68881 chip's addresses within the macros. The modification involves changing the 68881 from a data-space to a CPU-space device in the 68020-based computer. You must also make the 68000 math-operation macro library available to your software-development system.

To maintain object-code compatibility when moving up to a 68020 CPU, consider using the F-line trap technique, which, as noted earlier, forces the 68000 CPU into an exception state whenever it detects a coprocessor op code. First, use the math coprocessor's op codes in your program as if you were writing it for a 68020 computer. Second, design the interface circuit so that the 68881 chip operates as a peripheral in the 68000 supervisory program's address space.

You can use the F-line trap technique whether your 68000-family computer provides user and supervisory address space or a combined address space, but you'll need different software for each (**Fig 3** and **Listings 2** and **3**, pg 184). When you separate the user and supervisor address spaces, the 68000 operates in the protected mode. In the unprotected mode, the computer allows you to access the user's address space from within the supervisory program. The sample programs support all of the move-in transfer operations, but the routines don't check for errors or exceptions. If you need these operations, you can add them after you're sure the basic routines operate properly.

If you use the F-line trap routine to parse the 68881's coprocessor instructions and to determine the addressing mode, you'll slow the computer. To help overcome the overhead of fully decoding the addressing modes (ie, direct, indirect, indexed, displaced), the sample F-line trap routines let you use only the register-indirect addressing mode (A0). If you need more flexible addressing capabilities, load the effective address into the A0 register with an LEA EA,A0 command before you execute a floating-point instruction. Keep in mind that the LEA instruction assumes its operand is in a data space when you use program-counter-relative (PC-relative) addressing in a computer system that divides address spaces.

The F-line trap routines don't check the response register's contents for a null-come-again condition after they perform the final data transfer. The time the computer takes to execute a return-from-exception-condition (RTE) instruction is sufficient to ensure that no spurious protocol errors occur between sequential floating-point operations.

Listings show key program steps

When you use the unprotected version of the F-line trap routine **(Listing 3)**, the CPU detects coprocessor op codes and then goes into an exception state. While entering an exception state, the CPU saves the program counter's contents and processor status information on the stack. The trap routine then uses the program-counter value (PC) to locate the coprocessor instruction that caused the exception condition.

The trap routine compares the coprocessor op code

The 68881 lets you selectively enable or disable individual exception bits so your software monitors only the ones you choose.

TABLE 2—COMPARISON OF CLOCK-CYCLE REQUIREMENTS FOR MACRO AND F-LINE TRAP ROUTINES

OPERATION (MC68881)	MACRO SOFTWARE	F-LINE SOFTWARE PROTECTED	F-LINE SOFTWARE UNPROTECTED
F <op>.B <EA>, FPn	88	410	342
F <op>.W <EA>, FPn	88	410	342
F <op>.L <EA>, FPn	96	462	398
F <op>.S <EA>, FPn	96	462	398
F <op>.D <EA>, FPn	124	516	436
F <op>.X <EA>, FPn	156	570	474
F <op>.P <EA>, FPn	156	570	474
F <op>.X FPm, FPn	40	296	236
FMOVECR #ccc, FPn	40	370	316

<op> = MOVE, ADD, SUB, ETC.

with a 16-bit pattern at line 25 to test for the presence of a general-type op code. If the op code represents a general-type instruction and contains coprocessor address 1, the program fetches the coprocessor command word instruction from the address, (PC)+2, which follows the coprocessor op code. From lines 30 to 32, the trap routine loads the command word into the 68881's command register and puts the CPU into a null-come-again loop until the 68881 is ready for the next operation.

When the math chip is ready for the next command, the instructions at lines 33 and 34 dissect the command word to determine whether or not it requires multiple-register transfer operations. If such operations are needed, the routine branches to the GEN1XX location in the program. The sample program doesn't include the steps for multiple data-transfer operations, which are beyond this article's scope.

The instruction at line 35 tests for a floating-point register-to-register operation, which doesn't require any further operations in the trap routine. The instructions at lines 37 and 38 transfer control to address GEN011 if the program detects an instruction that moves information from the 68881 chip to memory. The sample trap routines support only the memory-to-68881 transfer operations, but you can use a similar trap routine to perform the 68881-to-memory data-transfer operations. The sample routine uses the ADD.W instructions to double the D1 register's value and set CPU flags. The addition has the effect of shifting the bit pattern one bit to the left.

The trap routines support the long-word, packed-BCD, and double- and extended-precision math operations (lines 54 to 56), and they handle both byte (lines 59 and 60) and word (lines 63 and 64) transfers. After the exception-trap routine transfers information to the math chip, it executes a return-from-exception instruction and transfers control back to your main program. Each of the F-line trap routines includes steps that save your working registers at the start of the routine and then restore them after the routine finishes working with the math chip.

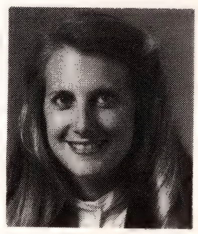
Because the F-line trap technique lets you use your software directly with a 68881 wired as a 68020 coprocessor, as well as with a 68881 wired as a peripheral for a 68000 chip, the trap technique has an advantage over the macro software technique. If, however, you don't plan to transfer your programs to a 68020 computer, you'll find that the macro routines run faster because they don't have to interpret coprocessor instructions each time one occurs in your program **(Table 2)**. **EDN**

References

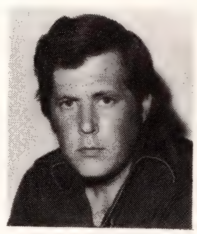
1. Harman, T, and Lawson, B, *The Motorola MC68000 Microprocessor Family*, Prentice-Hall Inc, Englewood Cliffs, NJ, 1985.

2. Motorola Inc, *MS68020 32-Bit µP User's Manual*, Prentice-Hall Inc, Englewood Cliffs, NJ, 1984.

Authors' biographies



Sarah Harris works as an electrical engineer in Motorola's memory design division in Austin, TX. Sarah is a graduate of Texas A and M University where she obtained a BSEE degree. Her hobbies include gourmet cooking, photography, and jogging.



Tom Johnson is a staff engineer whose duties include technical marketing and field communications. Tom works for Motorola in Austin, TX, where he is part of the high-end microprocessor division. During his nonworking hours, he enjoys photography and riding his horses.

Article Interest Quotient (Circle One)
High 482 Medium 483 Low 484

LISTING 1

```
************************************************************
*
*  MC68881 WORD IN MEMORY OR IN Dn TO FP-REG. OPERATION
*  MEMREGW   FUNCTION,<EA>,FPN
*  WHERE:  FUNCTION= FP INSTRUCTION MNEMONIC (I.E. FADD)
*          <EA>= SOURCE ADDRESSING MODE
*          FPN= DESTINATION REGISTER
*  NO REGISTERS MODIFIED OR DESTROYED!
*  VALID ADDRESSING MODES:
*          DN, (AN), (AN)+, -(AN), D(AN), D(AN,IX)
*          XXX.W, XXX.L, (D,PC), D(PC,IX)
************************************************************
MEMREGW   MACRO
          IFC '\4',''                         IS <EA>=INDIRECT WITH INDEXING
          MOVE.W #$5000+(\3<<7)+\1,MC6881+COMMAND
\@NULCA   CMPI #$8900,MC68881+RESPONSE        READ RESPONSE REGISTER
          BEQ.S    \@NULCA                    REREAD UNTIL EVAL EA AND
*                                             TRANSFER DATA
          MOVE.W \2,MC68881+OPER              WORD DATA TO FP-REG.
\@NULREL  TST.B MC68881+RESPONSE              IS RESPONSE NULL RELEASE?
          BMI.S \@NULREL                      BRANCH UNTIL NULL RELEASE
          ENDC
          IFNC '\4',''                        IS <EA> NOT=INDIRECT WITH INDEXING
          MOVE.W #$5000+(\4<<7)+\1,MC68881+COMMAND
\@NULCA   CMPI #$8900,MC68881+RESPONSE        READ RESPONSE REGISTER
          BEQ.S    \@NULCA                    REREAD UNTIL EVAL EA AND
*                                             TRANSFER DATA
          MOVE.W \2,\3,MC68881+OPER           WORD DATA TO FP REG.
\@NULREL  TST.B MC68881+RESPONSE              IS RESPONSE NULL RELEASE?
          BMI.S \@NULREL                      BRANCH UNTIL NULL RELEASE
          ENDC
          ENDM
```

LISTING 2

```
************************************************************
*
*   THIS CODE PERFORMS ONLY THE FUNCTION OF THE (AO)
*   MACRO EQUIVALENT!
*
*     *****MC68000 AND MC68010 UNPROTECTED VERSION*****
*
*   NO CHECKING IS DONE FOR ILLEGAL FORMAT ERRORS OR
*   COPROCESSOR DETECTED
*   EXCEPTIONS!
*
************************************************************
NUMREGS   EQU       2          NUMBER OF SAVED REGISTERS


MC68881   EQU       $838000    ADDRESS OF MC68881
OPERAND   EQU       $10        MC68881 OPERAND REGISTER
COMMAND   EQU       $0A        MC68881 COMMAND REGISTER
RESPONSE  EQU       $00        MC68881 RESPONSE REGISTER

```

Continued on pg 189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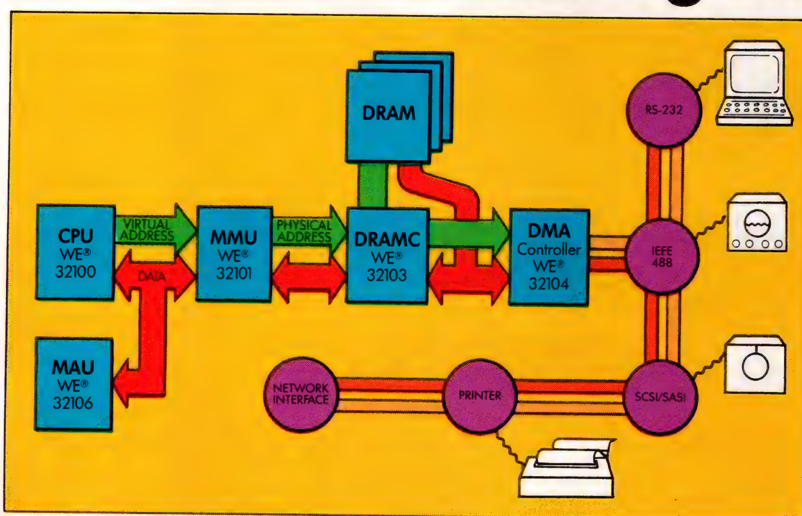

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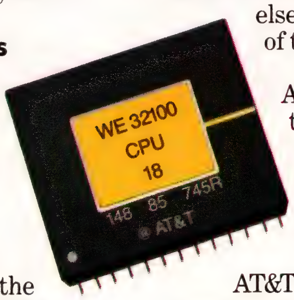

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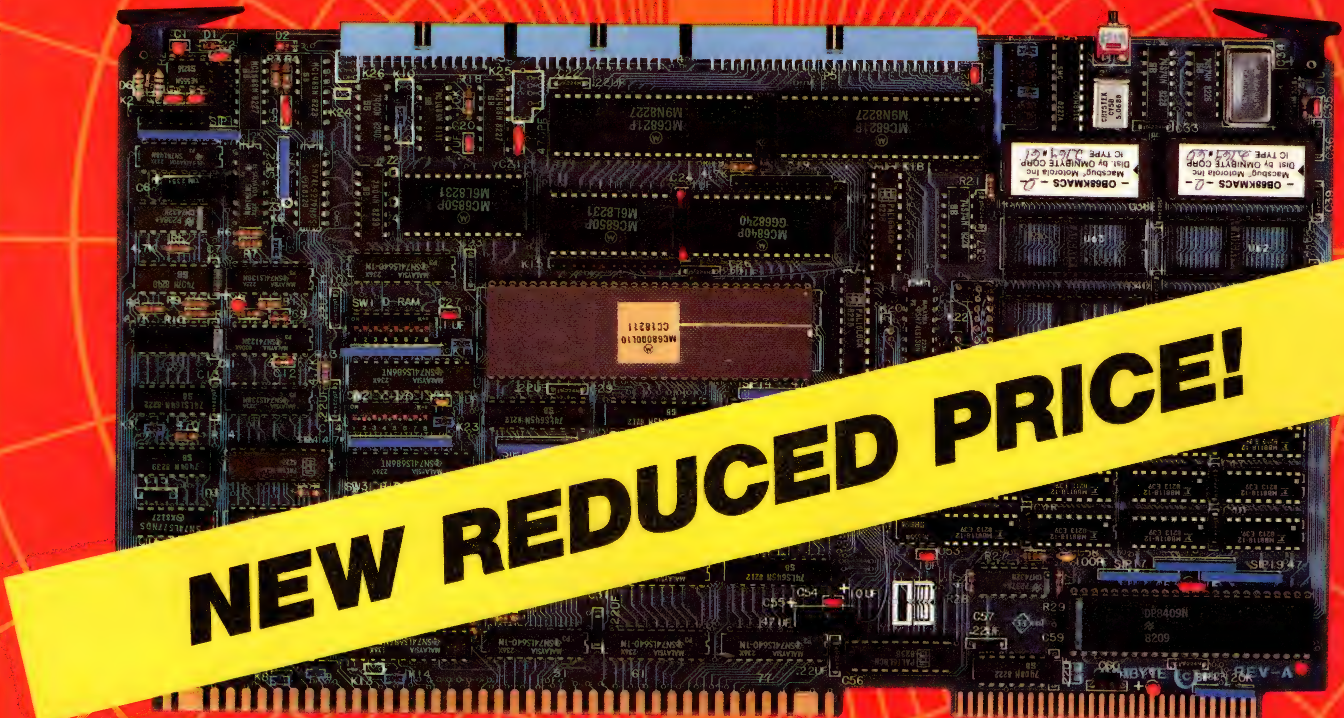

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CIRCLE NO 91

```
* FLINE ENTERS HERE...
FLINE    MOVE.L    A1,-(SP)  SAVE A1
         MOVE.L    D1,-(SP)  SAVE D1
         MOVE.L    NUMREGS*4+2(SP),A1 A1=USER PC
         MOVE.W    (A1)+,D1  D1 = OPCODE WORD
         CMP.W     #%1111001001000000,D1  ? CPID=1 AND GENERAL TYPE
         BHS       NOTGEN    BR IF NEITHER

* GENERAL INSTRUCTION
         MOVE.W    (A1)+,D1   D1 = CP COMMAND WORD
         MOVE.W   D1,MC68881+COMMAND  PASS TO '881
FGENWAIT CMP.W  #$8900,MC68881+RESPONSE  ? IS 881 BUSY
         BEQ      FGENWAIT   LOOP IF SO TILL ITS READY
         ADD.W    D1,D1      BREAK DOWN HIGH TWO BITS
         BCS      GEN1XX     BR SPECIAL MOVES
         BPL      GEN00X     BR REG-REG (MUST BE 000)

         ADD.W    D1,D1      TST NEXT BIT
         BMI      GEN011     BR REG-MEM

* IS A MOVE IN GENERAL INSTRUCTION (INCLUDING FMOVECR)
         ROL.W    #5,D1      SHIFT TYPE INTO WORD ACCESS POSITION
         AND.W    #$000E,D1  ISOLATE JUST TYPE FIELD*2
         MOVE.W   SIZETBL(D1.W),D1 OBTAIN SPECIAL TRANSFER SIZE CODE
         BMI.S    GENTSPC    BR IF IS NONE, BYTE, OR WORD

* TRANSFER THE COUNT OF LONGWORDS
         MOVE.L   A0,-(SP)   SAVE USER'S A0
GENTINL  MOVE.L   (A0)+,MC68881+DATA    NEXT WORD IN
         DBRA     D1,GENTINL LOOP TILL DONE
         MOVE.L   (SP)+,A0   RESTORE SAVED REGISTER
         BRA      FINI       EXIT AS WE ARE DONE

* SPECIAL COUNT OF NONE (FMOVECR), BYTE OR WORD
GENTSPC  ADD.B    #2,D1      OFFSET TO -1,0,+1
         BMI.S    GENTW      BR WORD TRANSFER
         BNE.S    FINI       BR FMOVECR (NO TRANSFER)

* MOVE BYTE IN
         MOVE.B   (A0),MC68881+DATA    STORE BYTE
         BRA      FINI       EXIT

* MOVE WORD IN
GENTW    MOVE.W   (A0),MC68881+DATA   STORE WORD
         BRA      FINI       EXIT

* SIZE TABLE-LONGWORDS TO COPY EXCEPT FOR NONE=-1 BYTE=-2 WORD=-3
SIZETBL  DC.W   0   .L
         DC.W   0   .S
         DC.W   2   .X
         DC.W   2   .P
         DC.W  -3   .W
         DC.W   1   .D
         DC.W  -2   .B
         DC.W  -1   FMOVECR (NONE)

* UPDATE PC AND RETURN TO CALLER
FINI     MOVE.L   A1,NUMREGS*4+2(SP)  SAVE SCAN PC
```

```
           MOVE.L   (SP)+,D1   RESTORE WORK
           MOVE.L   (SP)+,A1   REGISTERS
           RTE                 RETURN TO INVOKER

* UNILLUSTRATED CODE HANDLERS
GENO11     EQU   *
GENOOX     EQU   *
GEN1XX     EQU   *
NOTGEN     EQU   *

           END
```

LISTING 3

```
***********************************************************
*
*   THIS CODE PERFORMS ONLY THE FUNCTION OF THE (AO)
*               MACRO EQUIVALENT!
*
*          *****MC68010 PROTECTED VERSION*****
*
*   NO CHECKING IS DONE FOR ILLEGAL FORMAT ERRORS OR
*   COPROCESSOR DETECTED EXCEPTIONS!
*
***********************************************************
NUMREGS  EQU      2           NUMBER OF SAVED REGISTERS
UPAS     EQU      2           USER PROGRAM FUNCTION CODE VALUE
UDAS     EQU      1           USER DATA FUNCTION CODE VALUE

MC68881  EQU      $838000     ADDRESS OF MC68881
OPERAND  EQU      $10         MC68881 OPERAND REGISTER
COMMAND  EQU      $0A         MC68881 COMMAND REGISTER
RESPONSE EQU      $00         MC68881 RESPONSE REGISTER
         ORG      $2000
* FLINE ENTERS HERE...
FLINE    MOVE.L   A1,-(SP)    SAVE A1
         MOVE.L   D1,-(SP)    SAVE D1
         MOVE.L   NUMREGS*4+2(SP),A1 A1=USER PC
         MOVE.L   #UPAS,D1    SET UP
         MOVEC    D1,SFC      USER PROGRAM ACCESS
         MOVE.L   #UDAS,D1    SET UP
         MOVEC    D1,DFC      USER DATA ACCESS
         MOVES.W  (A1)+,D1    D1 = OPCODE WORD
         CMP.W    #%1111001001000000,D1  ? CPID=1 AND GENERAL TYPE
         BHS      NOTGEN      BR IF NIETHER

* GENERAL INSTRUCTION
         MOVES.W  (A1)+,D1    D1 = CP COMMAND WORD
         MOVE.W   D1,MC68881+COMMAND  PASS TO '881
FGENWAIT CMP.W    #$8900,MC68881+RESPONSE  ? IS 881 BUSY
         BEQ      FGENWAIT    LOOP IF SO TILL ITS READY
         ADD.W    D1,D1       BREAK DOWN HIGH TWO BITS
         BCS      GEN1XX      BR SPECIAL MOVES
         BPL      GENOOX      BR REG-REG (MUST BE OOO)

         ADD.W    D1,D1       TST NEXT BIT
         BMI      GENO11      BR REG-MEM
```

MIL-STD-1553

Taking the best products and making them BETTER...

1

ARX 18553 Miniature Transceiver

The world's smallest transceiver for use in MIL-STD-1553A and B data transmission systems. It includes all the features characteristic of other Aeroflex transceivers in a hermetically sealed 18 pin double DIP case.

2

ARX 2432 Remote Terminal Unit

A complete dual redundant MIL-STD-1553B remote terminal (RTU) in a 2.1 by 1.9 in. hybrid package. It includes dual transceivers, wrap around test capability, handles all mode codes plus broadcast and interfaces to subsystem via bidirectional 32 word FIFO memory.

3

ARX 1555LP Bit Processor

Low power version of ARX 1555 Bit Processor provides improved response times, higher reliability and lower power consumption without reduction in digital load driving capability. Features encoder, decoder, wrap around self-test capability, fail safe time out and address recognition.

4

ARX 3232 Multi-Bus Transceiver

Suitable for use in McDonnell Douglas (MACAIR) data transmissions systems as well as MIL-STD-1553A and B. Enhancements include active filter in driver for sinusoid waveform, high efficiency low power consumption voltage output driver, vey low dynamic offset and low differential phase delay.

5

ARX 8553 Transceiver

Our worldwide best seller is suitable for MIL-STD-1553A and B data transmission systems. Receiver has multipole low pass filter to enhance S/N ratio and tight threshold control to meet noise test requirements. The high efficiency driver consumes less power.

6

ARX 28553 Dual Redundant Transceiver

Two completely isolated transceivers in one. Low power consumption, improved filtering and short circuit protection. For MIL-STD-1553A & B applications requiring dual redundancy in small space.

Aeroflex's Data Bus Signal Processing Hybrids.

South Service Road
Plainview, NY 11803

AEROFLEX
Laboratories Inc.

Tel: (516) 694-6700
TWX: 510-224-6417

CIRCLE NO 92

```
* IS A MOVE IN GENERAL INSTRUCTION (INCLUDING FMOVECR)
          ROL.W     #5,D1        SHIFT TYPE INTO WORD ACCESS POSITION
          AND.W     #$000E,D1    ISOLATE JUST TYPE FIELD*2
          MOVE.W    SIZETBL(D1.W),D1 OBTAIN SPECIAL TRANSFER SIZE CODE
          BMI.S     GENTSPC      BR IF IS NONE, BYTE, OR WORD
* TRANSFER THE COUNT OF LONGWORDS
          MOVEM.L   D2/A0,-(SP) SAVE USER'S A0 AND A WORK REGISTER
GENTINL   MOVES.L   (A0)+,D2     NEXT WORD IN
          MOVE.L    D2,MC68881+DATA    NEXT WORD OUT
          DBRA      D1,GENTINL   LOOP TILL DONE
          MOVEM.L   (SP)+,D2/A0 RESTORE SAVED REGISTERS
          BRA       FINI         EXIT AS WE ARE DONE
* SPECIAL COUNT OF NONE (FMOVECR), BYTE OR WORD
GENTSPC   ADD.B     #2,D1        OFFSET TO -1,0,+1
          BMI.S     GENTW        BR WORD TRANSFER
          BNE.S     FINI         BR FMOVECR (NO TRANSFER)
* MOVE BYTE IN
          MOVES.B   (A0),D1      LOAD BYTE
          MOVE.B    D1,MC68881+DATA   STORE BYTE
          BRA       FINI         EXIT
* MOVE WORD IN
GENTW     MOVES.W (A0),D1        LOAD WORD
          MOVE.W    D1,MC68881+DATA   STORE WORD
          BRA       FINI         EXIT
* SIZE TABLE-LONGWORDS TO COPY EXCEPT FOR NONE=-1 BYTE=-2 WORD=-3
SIZETBL   DC.W   0   .L
          DC.W   0   .S
          DC.W   2   .X
          DC.W   2   .P
          DC.W  -3   .W
          DC.W   1   .D
          DC.W  -2   .B
          DC.W  -1    FMOVECR (NONE)
* UPDATE PC AND RETURN TO CALLER
FINI      MOVE.L    A1,NUMREGS*4+2(SP)  SAVE SCAN PC
          MOVE.L    (SP)+,D1     RESTORE WORK
          MOVE.L    (SP)+,A1     REGISTERS
          RTE                    RETURN TO INVOKER
* UNILLUSTRATED CODE HANDLERS
GEN011    EQU    *
GEN1XX    EQU    *
GEN00X    EQU    *
NOTGEN    EQU    *
          END
```

New 39C00 family!

Replace 2901Cs, 2910As with high-performance CMOS

Introducing drop-in replacements for the 2901C 4-bit microprocessor slice and 2910A 12-bit sequencer.

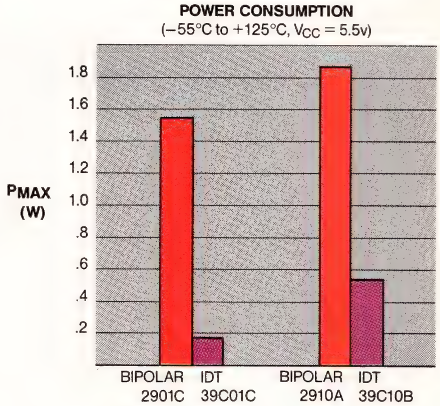
Same speed and output drive at CMOS power levels.
You now have a choice—bipolar 2900 or IDT's new 39C00 MICROSLICE™ family using the same instruction set as the fastest 2900 bipolar devices.

Use the IDT39C01C 4-bit microprocessor slice to replace the 2901C with a same-speed, equal-output drive, CMOS cool, pin-compatible and functionally equivalent device.

Use the pin-compatible IDT39C10B 12-bit sequencer to replace the 2910A and gain the performance and flexibility of a 33-deep stack.

Our advanced CEMOS™ II 1.2μm technology makes possible this unique combination of high-performance and low-power.

Availability. Both commercial and military product from stock packaged as 44-pin LCCs and 40-pin DIPs.



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Innovative bit-slice architectures

The world's biggest 2910A.

IDT's 49C000 CEMOS MICROSLICE family sets a new standard in high-performance bit-slice microprocessor products.
Extending the features of bit-slice to make possible more advanced designs. Providing architectural advancements and higher levels of integration.

Think of the IDT49C410 16-bit sequencer as an expanded version of the 2910A. The IDT49C410 brings about an immediate improvement in your overall system performance by providing a 16-bit address path—addressing 64K of microcode—plus a 33-deep stack and a 16-bit loop counter. Using the same microcode instruction set and operation codes you run on the 2910A.

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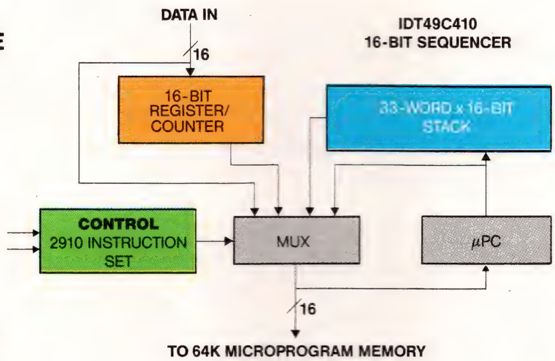

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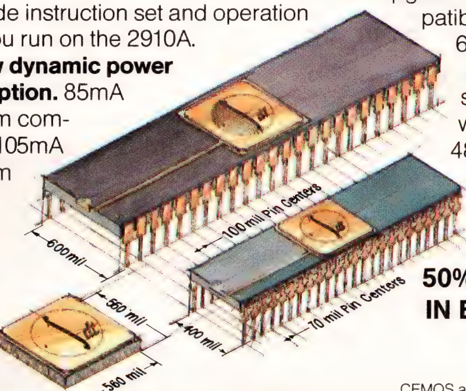
50% reduction in board space. Upgrades are easy with our pin compatible DIPs. Drop in the standard 600 mil 48-pin or cut board space in half with the space saving 400 mil wide DIP with 70 mil pin centers. Our 48-pin LCC provides even greater density.



50% REDUCTION IN BOARD AREA

The new force in bit-slice microprocessor products.
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CIRCLE NO 93

Floating-point array processor improves computational power

Powerful math-processing chips configured with high-speed memories and controllers form the core of a floating-point math or array processor for small computers. This second part of EDN's 3-part floating-point math series discusses the tradeoffs you must make to add flexibility and speed to array-processor designs.

Robert M Perlman, *Advanced Micro Devices*

For such jobs as digital-signal processing, image processing, graphics, and scientific calculations, an array processor can take over repetitive arithmetic chores while your host computer performs control tasks and retrieves information. By employing a floating-point array processor, you also increase the math-processing power of your computer system.

The basic array-processor design **(Fig 1)** contains an arithmetic unit, a controller, data memory, program memory, and a host interface (see **box,** "Array processor vs general-purpose computer"). If you use newer control, memory, and math chips, you can fit the circuit on a single pc board. This array-processor design uses an Am29325 floating-point processor chip, which operates with either IEEE- or DEC-standard single-precision data. The chip performs single-cycle floating-point additions, subtractions, multiplications, and format conversions at an 8-MHz clock frequency.

Because the Am29325 chip contains a floating-point arithmetic unit (AU), three 32-bit registers, two data buses, and two data-selection multiplexers, you need only a small amount of external hardware to design a complete math- or array-processor circuit. In the array-processor design, the Am29325 receives operands from two high-speed memories. An 8k×32-bit RAM provides input data for your algorithms, and it stores intermediate and final results. An 8k×32-bit PROM provides constant values for the algorithms.

Although you can design a circuit that specifically controls the math chip and its associated memory chips, you'll find an equivalent circuit in the 2910A microprogrammable controller chip. The 2910A chip is a general-purpose controller; it's not dedicated to controlling the Am29325. The controller chip contains a program counter, a loop counter, a LIFO stack, and other circuits that access program instructions and control the array processor in the basic design. The controller provides an 11-bit address for the design's 2k×64-bit microprogram memory, which contains the instructions for your algorithms. Each algorithm instruction con-

A basic array processor speeds math operations by performing repetitive tasks quickly.

tains 64 bits that the circuit divides into seven groups of outputs:

- 11 jump address bits
- one address and write-enable multiplexer bit
- one write-enable control bit
- 13 RAM-address bits
- 13 PROM-address bits
- 24 miscellaneous control bits
- one interrupt-control line.

The microprogram memory routes its outputs through an internal register and then to the rest of the array-processing hardware. Although it may not be obvious, the register at the microprogram memory's output helps maintain high-speed data processing. By using a clocked register to hold the memory's output bits, the controller latches a 64-bit instruction while it addresses the microprogram memory for the next instruction. The memory's output register therefore permits the overlap of the instruction-fetch and -execute operations, which saves processing time.

Because it holds information for a pending operation, the microprogram memory's output register is often referred to as a pipeline register. Array processors can contain a series of pipeline registers, the number of which depends on the architecture of the array processor and the maximum processing speed you need.

Host interface links processors

You must carefully choose your host-computer interface circuits according to the type of system bus in your computer. You can accommodate most general-purpose computers by providing bus buffers for the address,

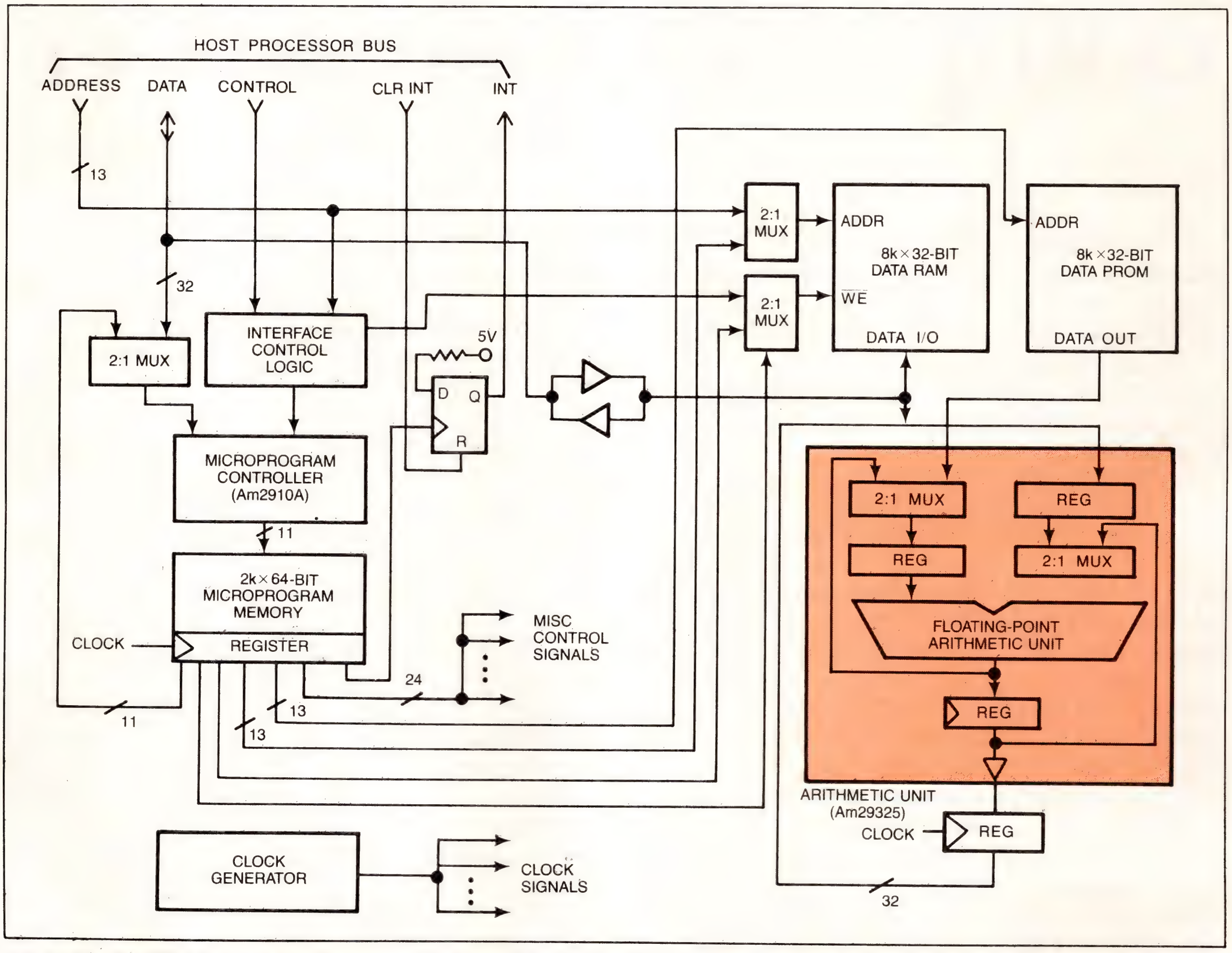


Fig 1—The Am29325 floating-point processor *used in this design adheres to IEEE and DEC floating-point standards.*

TABLE 1— BENCHMARK EXECUTION TIMES

OPERATION	EXECUTION TIME
5-TAP FIR FILTER	1.125 μSEC
RADIX-2 FFT BUTTERFLY	1.25 μSEC
4×1 MATRIX ADDITION	1.0 μSEC
4×4 MATRIX MULTIPLICATION	14.0 μSEC

data, and control lines. You'll also need a small amount of control logic to manage the flow of information to and from the array processor and the host computer. For example, you can construct a Multibus interface by using octal bus buffers and PAL chips. If your host computer's data bus contains fewer than 32 data bits, you'll need to convert the data to and from the 32-bit format that the array processor requires. You can include double-buffer latch circuits for the data inputs to the array processor, and you can provide latches and multiplexers on the processor's data-output lines.

The host computer's data bus provides the main link between the host and the array processor. Your computer starts a math operation by loading the RAM with raw data and then signaling the array processor to start a math-processing algorithm. After the processor runs an algorithm program, your host computer reads the RAM's contents to obtain the results.

To simplify the data-transfer operations to and from the host computer, the array processor goes into an idle, or standby, state when it isn't running an algorithm program. Instead of controlling the processor's data and control lines, the microprogram controller continuously runs a 1-microinstruction program loop. In addition, the idle microinstruction switches the RAM's address and write-enable multiplexers so that the RAM appears to be part of the host computer's main memory. The host computer loads the desired input data into the data RAM, and it then loads the microprogram controller with the starting address of the algorithm you want to run. The microprogram controller then jumps to the preprogrammed sequence of microinstructions for the algorithm. The algorithm's first microinstruction reconfigures the data RAM so that only the array processor can address it. When the algorithm completes its tasks, it sends an interrupt signal to the host processor, switches the data RAM back to the host, and executes the 1-instruction standby loop.

Once you're sure the array processor is operating properly, you can test the operating speed of your circuit by using benchmark programs tailored to specific tasks **(Table 1).** The benchmark times were calculated for the array processor with an 8-MHz clock frequency. The basic processor performs one data-RAM operation (read or write) per clock cycle.

Modifications improve performance

Although the basic array-processor circuit works well, you can improve its performance. The ability to take data addresses directly from the program memory in the simple array processor means that the program memory must contain a section of microcode for each iteration of an algorithm. For example, a program that performs 20 matrix multiplications contains a separate section of microprogram code for each multiplication

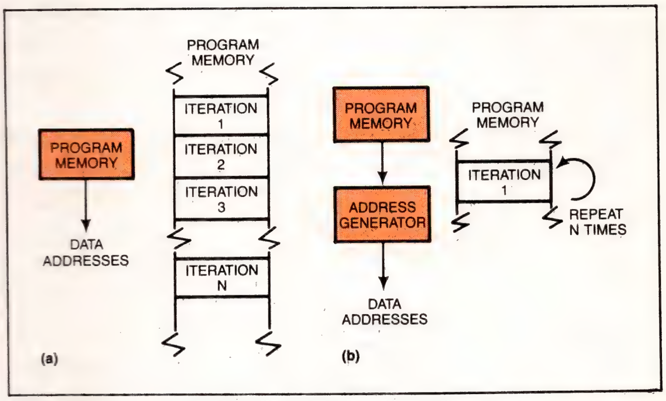


Fig 2—You can implement the program memory in two ways: *Either you can include steps for each iteration of your algorithm* ***(a)****, or you can add an address-generator circuit* ***(b)*** *that lets you use only one section of code for all iterations. The address generator locates specific values and coefficients in memory automatically.*

step. Each code section contains specific addresses for data and coefficients **(Fig 2a).** The in-line coding approach therefore wastes program-memory space.

One improvement found in virtually every array processor is a data-address-generator circuit that generates the necessary data and coefficient addresses within the array processor. The address-generator hardware reduces the amount of microprogram memory you'll need for an algorithm. By using such hardware, the processor performs multiple iterations of an operation by looping through the same section of microcode as many times as necessary **(Fig 2b).**

Depending on your specific tasks, you can choose a data-address generator that fits a specific algorithm, such as the fast Fourier transform (FFT), or you can choose a general-purpose addressing device. Some

Text continues on pg 200

Array processor vs general-purpose computer

To understand better what an array processor does, consider first the strengths and shortcomings of general-purpose computers. General-purpose computers incorporate the standard Von Neumann architecture and perform a variety of tasks. Such computers perform instruction-fetch and instruction-execution tasks sequentially, with instructions and data available in one memory array **(Fig A)**.

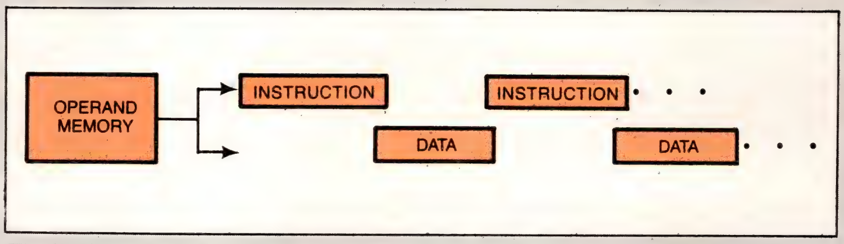


***Fig A—A general-purpose computer memory** stores instructions and data in the same block. The computer must access instruction and data values sequentially.*

Consider the calculation of the sum of products, a common task in signal-processing and matrix-manipulation algorithms. The basic sum-of-products equation is

$$Y = \sum_{i=1}^{N} k_i x_i,$$

where k_i and x_i represent coefficients and data stored in memory, respectively. The sum-of-products computation represents a large class of array-processing problems that share three fundamental characteristics: First, they involve repetitive computations on arrays of data. Second, the underlying control structure is simple, having many loops but no conditional branches. Third, the math steps are memory-intensive—each calculation requires one data point and one constant from memory.

To evaluate a product term, the computer fetches x_i and k_i, multiplies them, and then adds the result to the running total. Each step requires an instruction-fetch cycle and an instruction-execution cycle. Although specific details vary from computer to computer, in general even primitive math operations require many cycles.

Overlapping operation

Traditionally, Von Neumann-type computers perform each step sequentially. Array processors, however, provide a degree of parallelism by doing more than one thing at a time. When data and program steps reside in separate memories—an arrangement that fits the Harvard-architecture model—instruction- and data-fetch operations can overlap **(Fig B)**. In the case of the sum-of-products operation, the array processor fetches the input operands at the same time that it fetches the instruction that performs the multiplication. Most array processors also overlap instruction-fetch and instruction-execution operations.

For highly regular, math-intensive algorithms, the overlapping results in high-speed operation, but such operation can be inefficient when the algorithm includes conditional branches. If, for example, a program calls for a conditional branch to another instruction, the instruction following the branch instruction may be in the instruction queue. If it is in the queue, the computer discards it. Array processors are therefore best suited to the many number-crunching algorithms that require little or no conditional branching.

Because array processors provide parallel operation, you can optimize them for a specific math process. For example, an array processor designed for a sum-of-products operation may contain a multiplier and adder circuit, which evaluates a product term in one cycle. Because array processors perform parallel operations, programming the processors is more demanding than programming a general-purpose computer. However, the resulting increase in computational power often justifies the additional programming effort. Instead of programming in Basic or in assembly language, you'll use a microcode that controls individual circuits and operations in the array processor. Although such programming is demand-

ing, it gives you complete control of the array processor's internal operations.

Five functional blocks

Array processors typically receive data and instructions from a host machine—usually a general-purpose computer. Although specific array-processor architectures vary greatly, most processors contain at least five functional blocks: an arithmetic unit, data memory, a controller, program memory, and a host interface.

The heart of the processor is the arithmetic unit, which controls the data paths and performs arithmetic operations. Depending on your application, the arithmetic unit performs fixed-point operations, floating-point operations, or both. For some high-speed, real-time applications, such as radar- and video-information processing, array processors operate on 12-, 16-, or 24-bit fixed-point data. However, the trend is toward 32-bit floating-point data processing.

The data-memory—usually banks of high-speed RAM or PROM—supplies operands to the arithmetic unit and stores results from the arithmetic unit. The data memory can have multiple data ports, depending on how fast the memory chips must supply operands and accept results. If it doesn't have enough ports or enough speed, the data memory can become a processing bottleneck, leaving the arithmetic unit starved for operands.

Controller is simple

The controller sequences the array processor through its operations. Because most array-processing algorithms have modest sequencing requirements, the controller isn't complex. Controllers provide a program counter (PC) that you increment to access the next program-memory word. You can also load the PC with the program memory's output to force the controller to jump to a different part of the program. The controller includes a loop counter, which counts repeated operations. Depending on the array processor's sophistication, the controller may incorporate circuits that control nested subroutines, interrupts, and conditional-branch operations.

The program memory stores the array processor's microcode, which controls the other processor elements. Like the data memory, the program memory can be RAM or PROM. Use PROMs when the algorithms are well-defined and unlikely to change. Use RAM during algorithm development. The resources in the array processor determine the microcode memory's bit width. For example, a 60-bit-wide program memory provides 30 bits that control the arithmetic unit, 15 bits that transfer information to the controller (including a 12-bit jump address), and 15 bits that control other internal array-processor resources.

The host interface transfers data and instructions between the host computer and the array processor—usually by DMA operations. The host computer sends the array processor a block of data and an instruction word that selects a processing algorithm. After processing the data, the array processor transfers the results to the host computer.

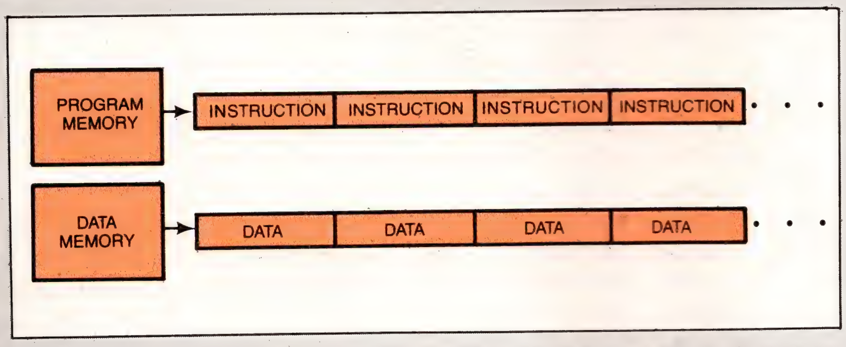


Fig B—An array processor's memory provides separate storage blocks for instructions and data. The separate storage areas let the control circuits access instructions and data in parallel.

An array processor can include pipeline registers that let the circuit overlap tasks.

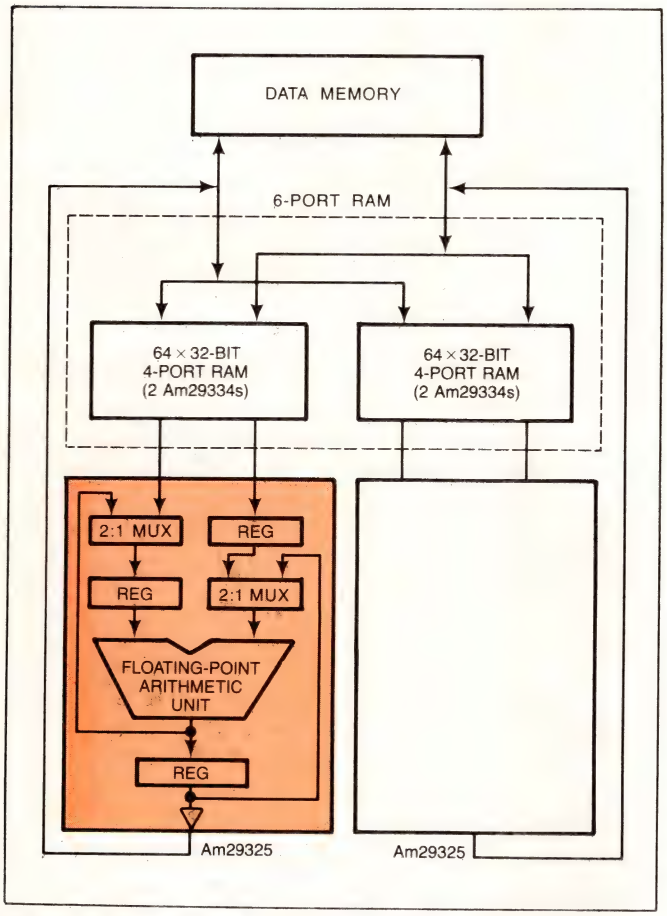


***Fig 3—A 6-port RAM speeds data transfers** so that two math-processor chips can operate independently. The chips can process data from the memory or from one another.*

array processors provide both a general-purpose and a dedicated address-generator circuit. You'll find separate address generators for data and coefficient memories in array processors that provide extremely high processing speeds.

An address generator reduces the size of your array processor's program memory, and it increases the processor's speed. To increase processing speed further, consider adding arithmetic hardware to your design so the processor can do several computations in parallel. In the basic array-processor design, the arithmetic unit performs one operation at a time—for example, sums of products, which involve alternate addition and multiplication operations. The array processor performs the multiplication and addition operations sequentially.

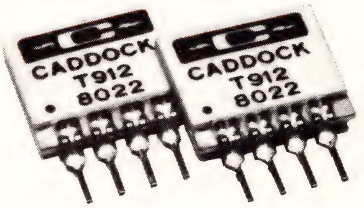
The throughput of the basic array processor is 250 nsec per floating-point product term; to increase that speed you can gang two 29325 floating-point math processors **(Fig 3).** The processors communicate through a 6-port RAM. When the circuit incorporates a multiport RAM, the floating-point processors can each access two input operands and store one result during each clock cycle. Because data produced by one floating-point processor is accessible to the other, you can double the processing speed for such algorithms as sum-of-products: One processor produces product terms, while the other processor sums and accumulates them. Of course, you can choose other math-chip configurations that better suit specific array-processing tasks. Keep in mind, however, that although you gain higher-speed operations by providing parallel math chips, your programming tasks grow. Coordinating the software operations of several parallel math chips can be difficult.

Memory expansion increases throughput

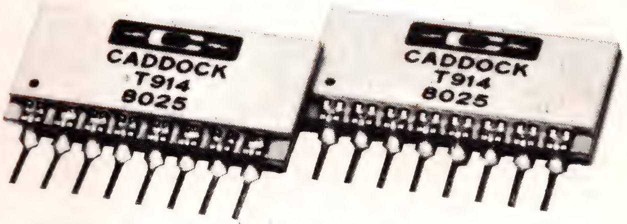
When you upgrade the arithmetic unit by adding parallel math chips, you must improve the data memory as well. The data-memory configuration in the basic array processor limits processing speed because the processor only accesses one constant and only performs one RAM-read or -write operation per clock cycle. To let the array processor perform operations that require two operands from RAM in the same cycle, or that require RAM-read and -write operations during the same cycle, you must upgrade the memory. Possible enhancements include converting the coefficient PROM to high-speed RAM, running the data RAM at twice the processor's speed to allow single-cycle reading and writing, or replacing the data RAM with a 2-port RAM.

In addition to high processing speeds, some applications may require rapid data transfers between the array processor and the host computer. There are at least two ways of speeding the transfer of data from the host to the array processor. First, you can replace the array processor's data RAM with a 2-section memory **(Fig 4)** that gives the host computer access to one section while the array processor uses the other. When the array processor completes its task, it switches between the buffers. The host obtains the results from the array processor's old buffer, while the processor operates with the data in the host's old buffer. The host computer's and the array processor's operations are no longer sequential; instead, they overlap. You'll have to pay careful attention to the manner in which the array processor controls the 2-section memory, because you

Type T912 / T914 Ultra-Precision Resistor Networks from CADDOCK provide Ratio TCs to 2 PPM/°C and Ratio Tolerances to ±0.01% for precision analog designs.



Type T912 Ultra-Precision Resistor Network 'Pairs'

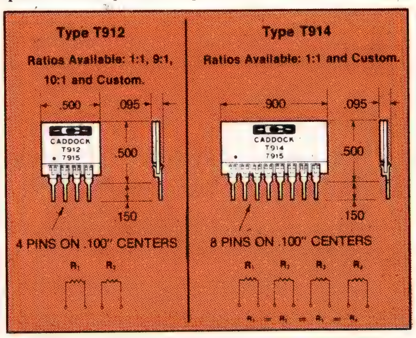


Type T914 Ultra-Precision Resistor Network 'Quads'

Type T912 / T914 Ultra-Precision Resistor Networks are constructed with Caddock's Tetrinox™ resistance films to achieve all of these high performance characteristics:

- **Absolute Tolerance:** 0.1% for all resistors.
- **Ratio Tolerances:** From ±0.1% to ±0.01%.
- **Ratio Temperature Coefficients:** From 10 PPM/°C to 2 PPM/°C.
- **Absolute Temperature Coefficient:** ±25 PPM/°C from 0°C to +70°C, referenced to +25°C.
- **Ratio Stability of Resistance at Full Load for 2000 Hours:** Within ±0.01%.
- **Shelf Life Stability of Ratio for Six Months:** Within ±0.005%.

This exceptional combination of performance specifications – and the compact, plug-in configuration of the Type T912/T914 precision resistor 'pairs' and 'quads' – provide the single-package



matched resistor characteristics and stability required by high-accuracy analog circuits, including –

- **Precision analog amplifiers.**
- **Voltage reference circuits.**
- **Instrumentation bridge circuits.**
- **Voltage and current comparison circuits.**

Standard models of Type T912 / T914 precision resistor 'pairs' and 'quads' include 14 off-the-shelf resistor values with a wide choice of Ratio Tolerances, Ratio TCs and Resistance Ratios:

This standard part number provides a selection of over 500 in-production models of Type T912/T914 precision resistor 'pairs' and 'quads':

T912 - A 1K - 010 - 10

Model Number.

Ratio Code Letter:

A – T912 with $R_2 = 10R_1$ (Example: 1K – 10K)

B – T912 with $R_2 = 9R_1$ (Example: 1K – 9K)

No Letter – T912 with $R_2 = R_1$

No Letter – T914 with $R_1 = R_2 = R_3 = R_4$

Standard Resistance Values (R_1):

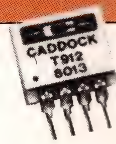
1K	10K	40K	200K	500K
2K	20K	50K	250K	1 Meg.
5K	25K	100K	400K	

Ratio Tolerance:

-100 = 0.1% -020 = 0.02%
-050 = 0.05% -010 = 0.01%

Ratio Temperature Track: (0°C to +70°C)

-10 = 10PPM/°C -05 = 5PPM/°C
-02 = 2PPM/°C



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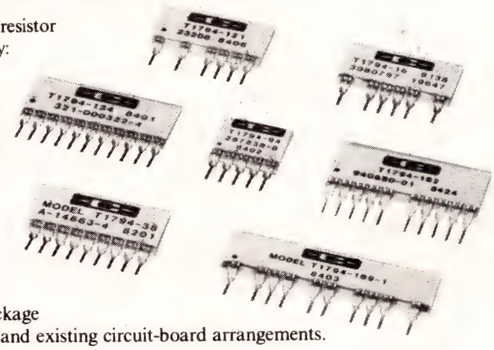

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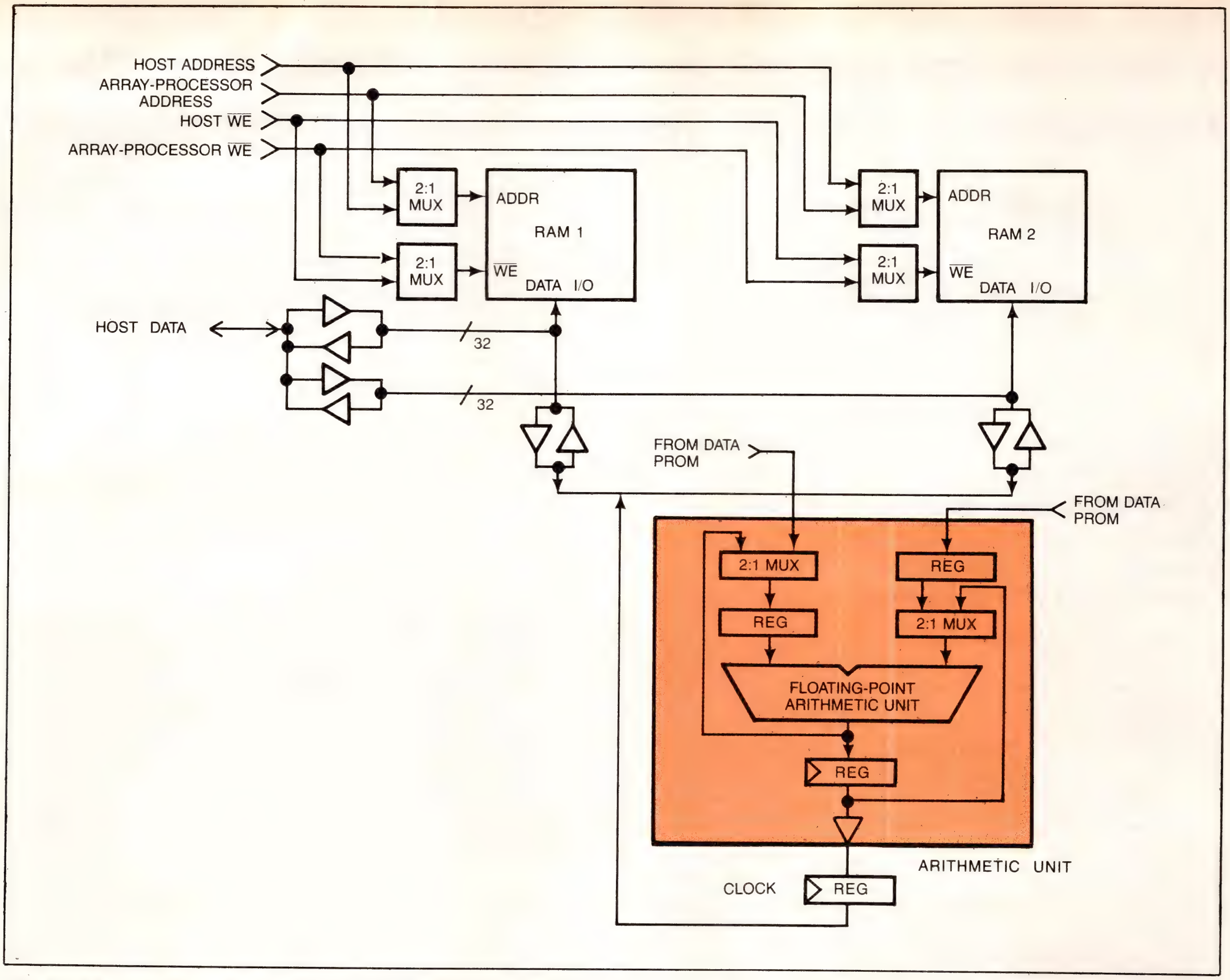

Fig 4—A 2-section memory offers a speed enhancement. *The host processor reads or writes from one section, while the array processor processes the data in the other section.*

don't want to switch buffers while the host or the array processor is still using one.

A second approach involves bypassing the host computer and letting the array processor take data directly from the data source—for example, an A/D converter. The processor uses the data and passes results to the host computer.

The 2-section-memory and direct-data-input techniques aren't mutually exclusive. In a given application, you might send data from an A/D converter directly to a 2-section memory. In this case, when the A/D converter's memory is full, it switches the memory section to the array processor.

Dividing the work load

By adding both direct-data input and output ports to your array-processor design, you can connect several processors in series, letting each one perform a subset of your algorithm. After it processes a piece or block of information, each processor passes results to the next processor in the chain.

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Author's biography

Robert M Perlman is the section manager for arithmetic accelerators at Advanced Micro Devices Inc (Sunnyvale, CA). Bob has been with AMD for 2½ years. His work involves developing and defining new products. He holds a BSEE from RPI, and he obtained his MSEE from Johns Hopkins University in 1981. Bob is an extra-class amateur-radio operator (KG6AF).

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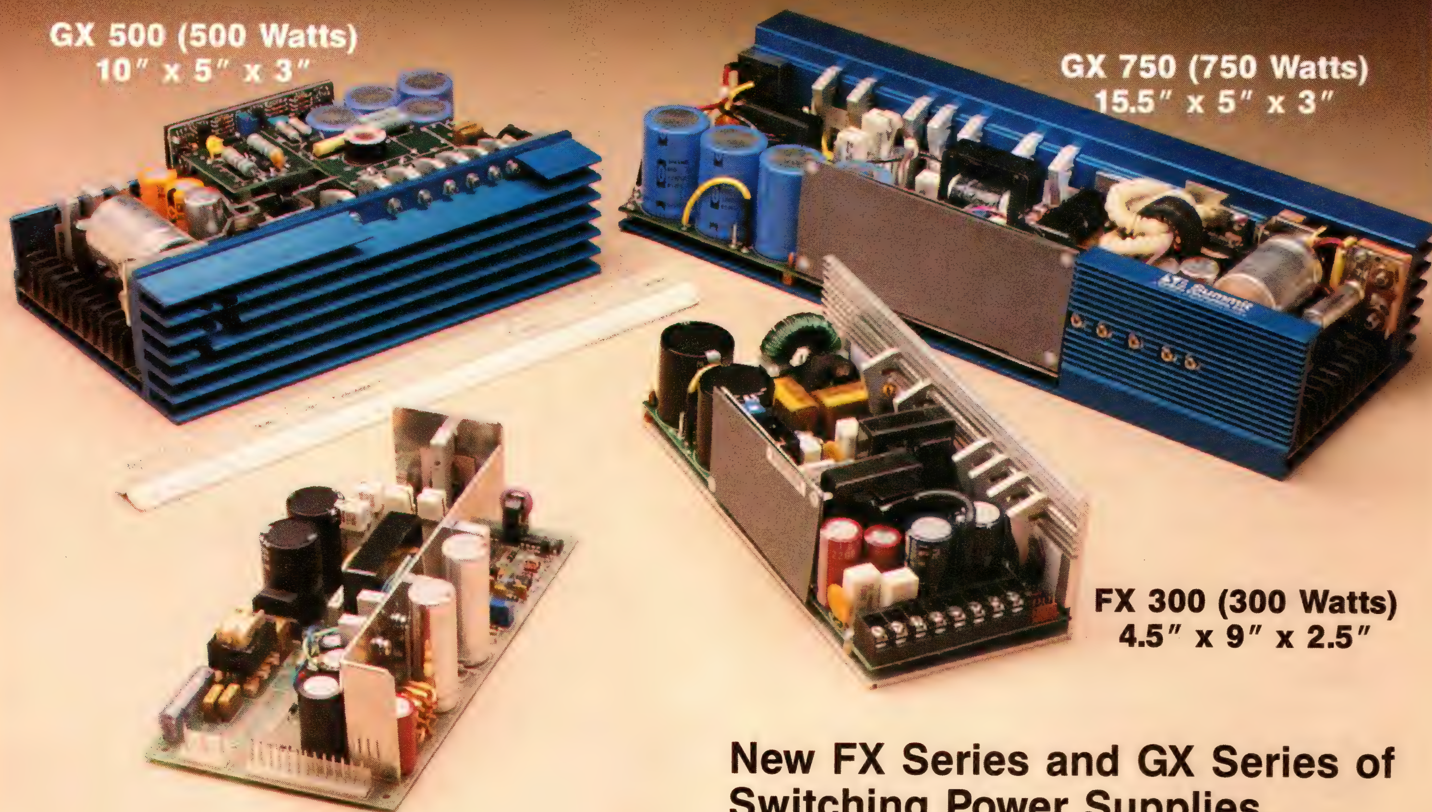

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CIRCLE NO 96

EDITED BY TARLTON FLEMING

Converters yield droop-free S/H circuit

T G Barnett
The London Hospital Medical College,
London, UK

In low-frequency applications, many monolithic sample/hold circuits suffer a droop rate that can cause an unacceptably large output error. The S/H circuit in **Fig 1** eliminates droop error by operating two 8-bit multifunction converters back to back. The circuit requires a 5V supply and accepts analog inputs between 0 and 2.5V (although you can scale and offset any input signal to fall within this range).

The analog input is applied to the inverting input of an LM324 op amp (IC_1), which is wired as a comparator. The op amp and the IC_2 multifunction converter form a ramp-and-compare A/D converter. (Because the Ferranti ZN435 multifunction converter includes a voltage-output D/A converter, an 8-bit up/down counter, a 2.5V bandgap reference, and a clock generator, you can configure the device either as an A/D or as a D/A converter.) The converter's internal counter counts from 0, producing a positive-going ramp at the analog output.

When the ramp voltage exceeds the analog input, the comparator output goes high and sets IC_5's Q_1 output high, thus inhibiting IC_2's clock and stopping the counter. IC_2's digital outputs are connected to the digital inputs of IC_3, which is wired as a D/A converter. The D/A converter provides the S/H circuit's analog output.

The output will remain in a hold state until you reset the monostable multivibrator (IC_4), whose outputs apply simultaneous reset pulses to IC_2 and IC_5. The circuit then resamples and holds a new value of analog input. The S/H circuit provides 8-bit hold accuracy for analog input frequencies as high as 1 kHz; you can use a faster op amp for IC_1 for higher-frequency operation. **EDN**

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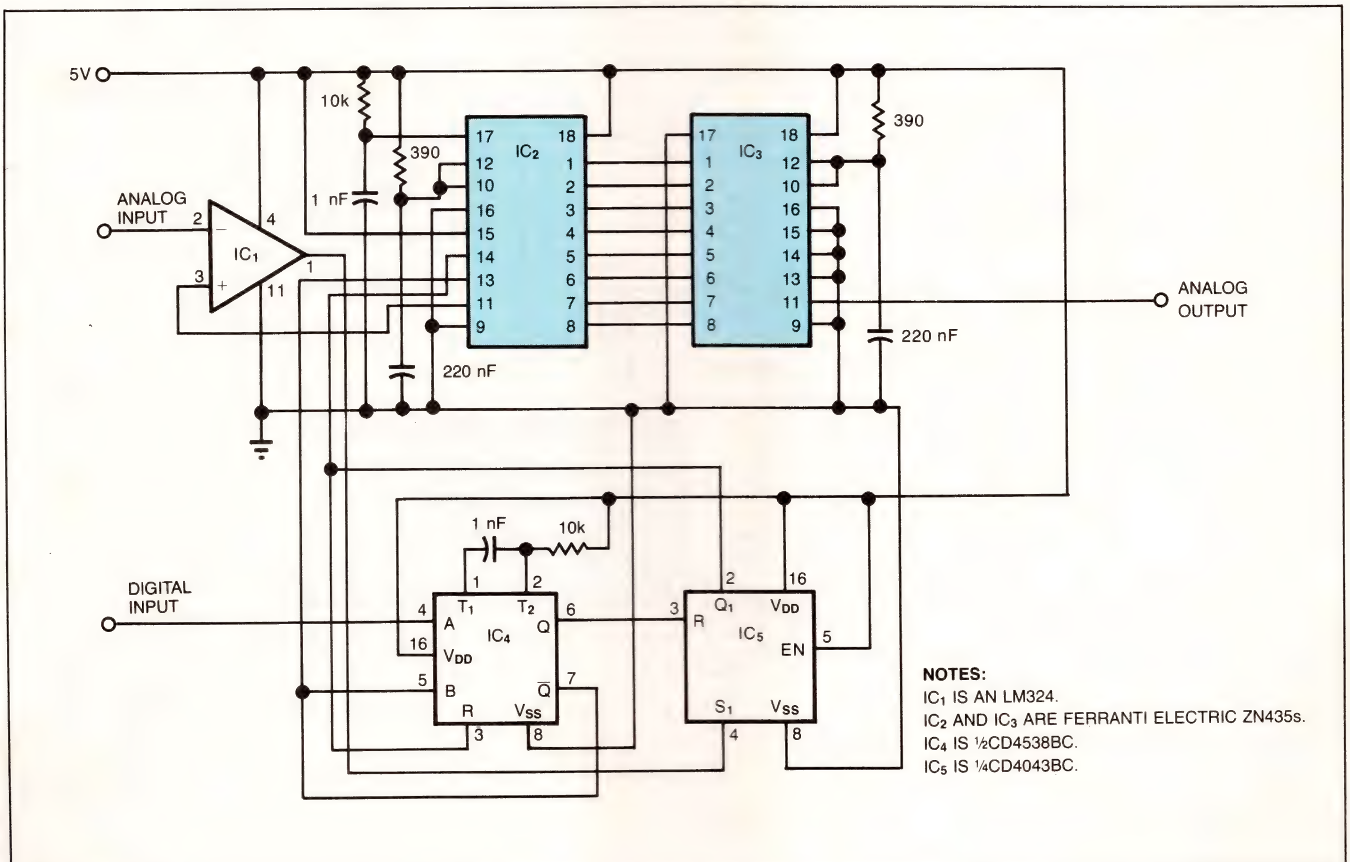

***Fig 1—This S/H circuit provides unlimited hold time** without droop by digitizing the analog input (IC_2) and converting back to analog using a D/A converter (IC_3).*

Enhance the 8214 interrupt controller

Dan G Sporea and Octavian C Cotescu
National Center of Physics,
Magurele 5206, Romania

The 8214 priority interrupt controller is intended for use with the Z80 μP operating in mode 0 and with the 8080 μP. You can use the 8214 with a Z80 operating in mode 2 by adding a 5-bit shift register (IC_3) to the classical 8214-8212 arrangement **(Fig 1)**.

An 8-bit word is assembled in IC_4's I/O port by adding the five bits from IC_3 to three bits from IC_2, forming an 8-bit priority-encoded interrupt vector corresponding to the highest-priority interrupt request at the 8214's inputs. (Using the PE and $\overline{CL}$ commands, you load the appropriate five bits into IC_3 before the program runs. For a Z80 running in mode 0, all of the bits are 1s.) The 8-bit vector is placed on the data bus during an interrupt-acknowledge cycle, when the 8212 is activated by the $\overline{IORQ}$ and $\overline{MI}$ signals.

You must program the interrupt-service routines according to the 8214's data sheet, but you should end each routine with a RET instruction instead of the RET1 instruction normally used with Z80-family peripherals.

The circuit offers the following advantages:

- You can obtain Z80 mode-2 operation for peripherals other than those intended for that purpose.
- You can dynamically reassign the interrupt-service routines by altering the word stored in IC_3's shift register.
- Using a word stored in another 8212 port, you can mask interrupt signals R_0 through R_7 so that only software-selected inputs are served.
- You can implement a daisy-chain priority-interrupt system with maskable inputs. **EDN**

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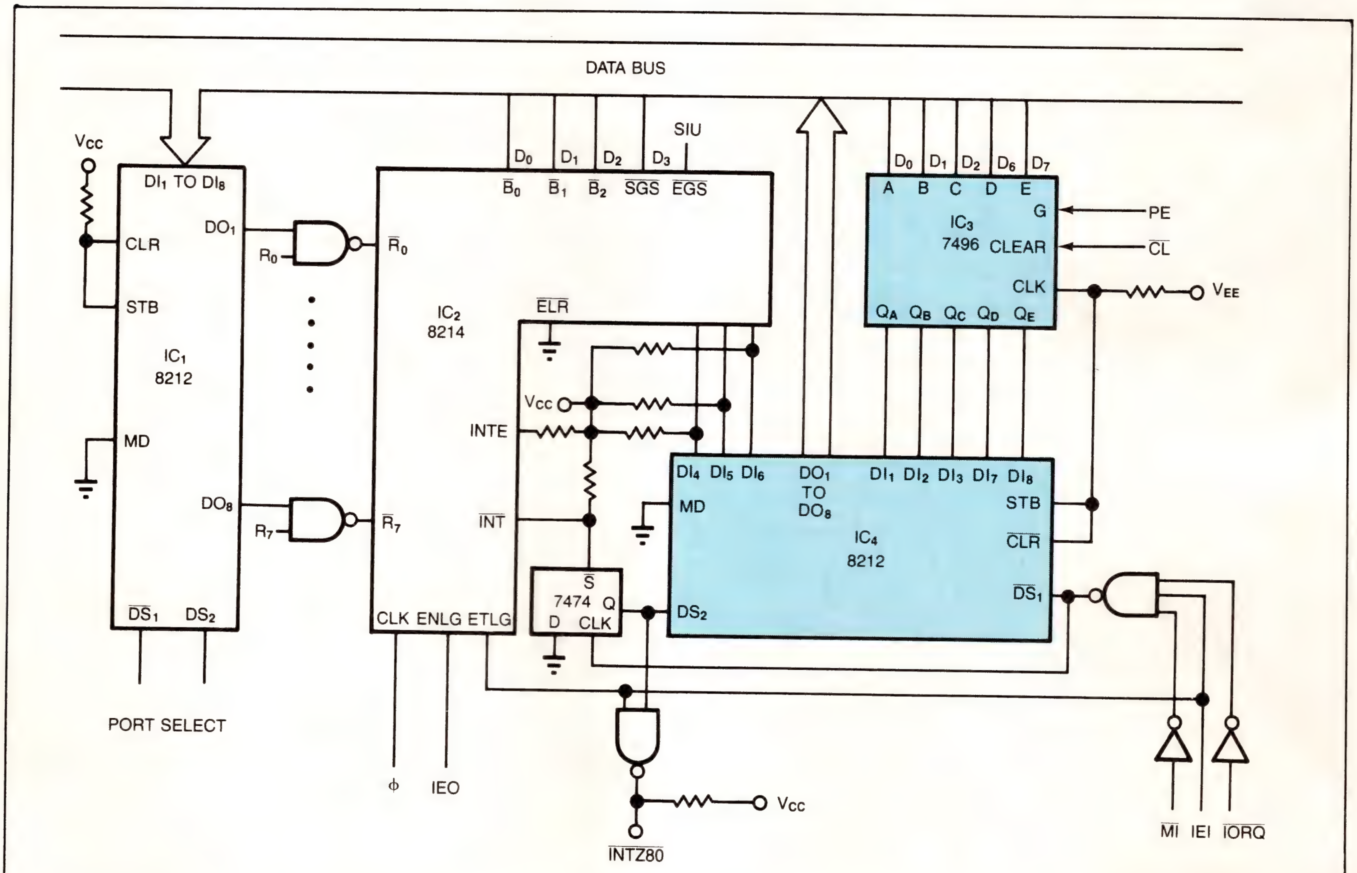

Fig 1—A more versatile interrupt-service capability and Z80 mode-2 operation are achieved by adding a shift register and I/O port (IC_3 and IC_4) to the usual 8214/8212 configuration.

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SBL-1-1	0.1-400	5.5	35	40	**$6.50**
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C104 REV. ORIG.

Serial pulses control analog multiplexer

Al Kumar
Simmonds Precision, ISD Div, Vergennes, VT

Using the **Fig 1** circuit, you can control an 8-channel analog multiplexer from a remote computer via a differential signal path. Binary counter IC_{3B} provides both a latch function for the channel address and the means for a sequential scan through the channels.

You control the multiplexer by negative-going pulses transmitted to the differential receiver IC_1. For the 50-kHz clock frequency shown, a wide pulse (200 to 250 μsec) sets the multiplexer to channel 1, and each additional short pulse (25 to 35 μsec) steps the multiplexer to the next channel in sequence. (The receiver output should maintain a logic-1 level between the pulses to clear counter IC_{3A} and stop its counting.)

Counter IC_{3A} begins counting when a long pulse arrives, causing the LSB output (line 3) to clock the IC_{3B} counter. The multiplexer, in turn, scans its eight channels in response to the count from IC_{3B}. The multiplexer will, however, stop on channel 1 because when pin 6 of IC_{3A} is high, it sets IC_{3B}'s outputs to 0s.

Short pulses, on the other hand, allow only enough time for completion of the first low-to-high transition on pin 3 of IC_{3A}. As a result, inverter IC_2 produces a negative edge at IC_{3B}'s clock, which increments that counter by 1 and selects the next multiplexer channel.

EDN

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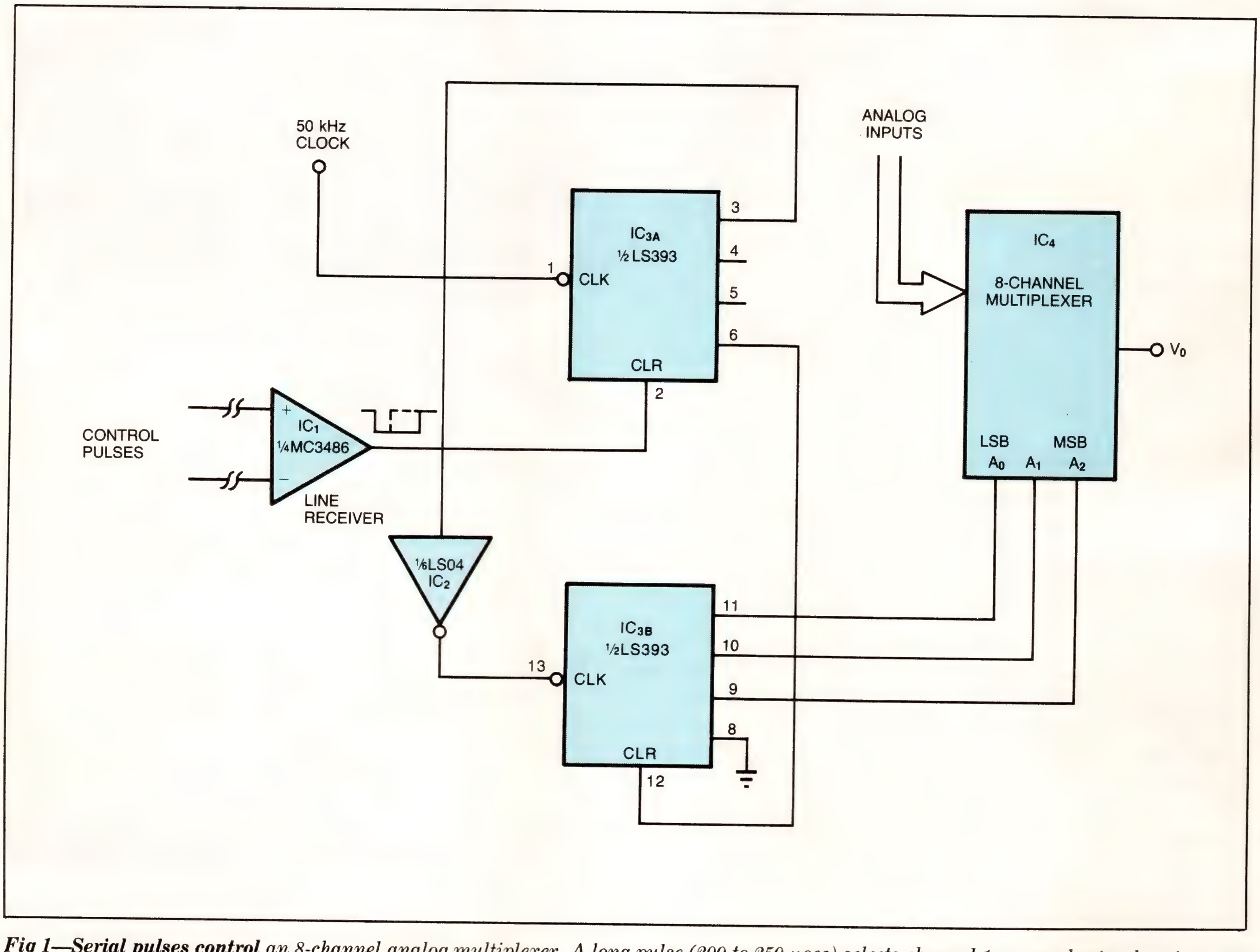

*Fig 1—**Serial pulses control** an 8-channel analog multiplexer. A long pulse (200 to 250 μsec) selects channel 1; seven short pulses (25 to 35 μsec) step the multiplexer through its remaining channels.*

Divider produces symmetrical output

Irwin Cohen
Hewlett-Packard Co, Rockaway, NJ

In synchronous systems, you must often divide a symmetrical clock waveform by an odd integer and obtain a symmetrical output (ie, a 50% duty cycle). Unfortunately, J-K flip-flop dividers usually produce a waveform (labeled A in **Fig 1b**) in which the high and low intervals differ by one period of the input clock. The **Fig 1a** circuit corrects this situation by splitting the difference—it lengthens the short interval and shortens the long one by half a clock period. The circuit works for any odd-integer division producing an asymmetry of one clock period; division by 3 is used as an illustration.

Flip-flop IC_3's Q output is set high when waveform A is low; Q goes low with the first positive transition of f_{IN} after A returns high (**Fig 1b**). If $T_1 > T_2$, connect IC_{1B}'s Q output instead of the $\overline{Q}$ output to IC_3's preset input.

EDN

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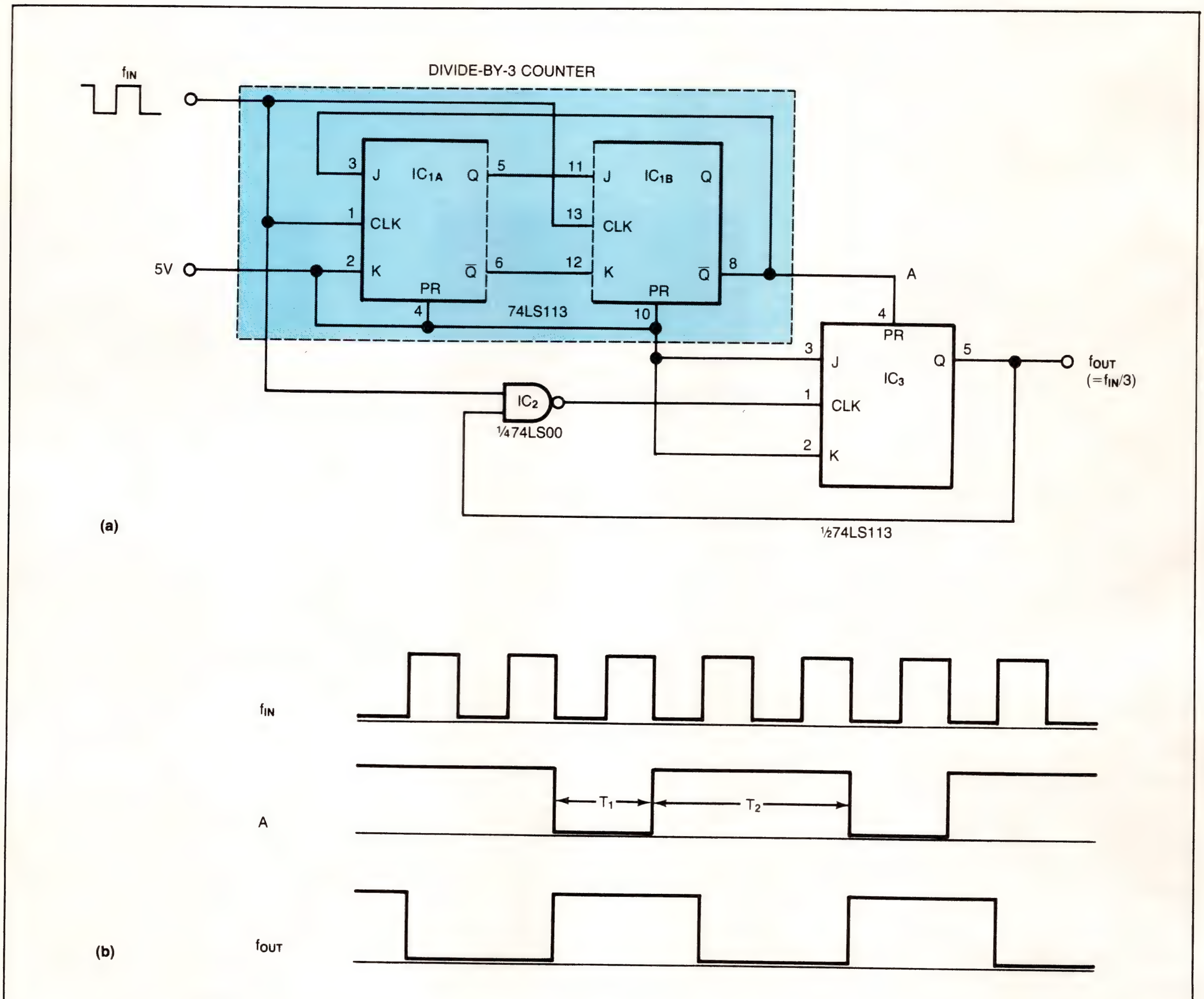

*Fig 1—**Odd-integer division** performed using a divide-by-3 counter **(a)** produces the asymmetrical waveform (such as the one labeled A in part **b**), but you can add additional circuitry to generate a symmetrical f_{OUT} signal.*

Decoupling IV

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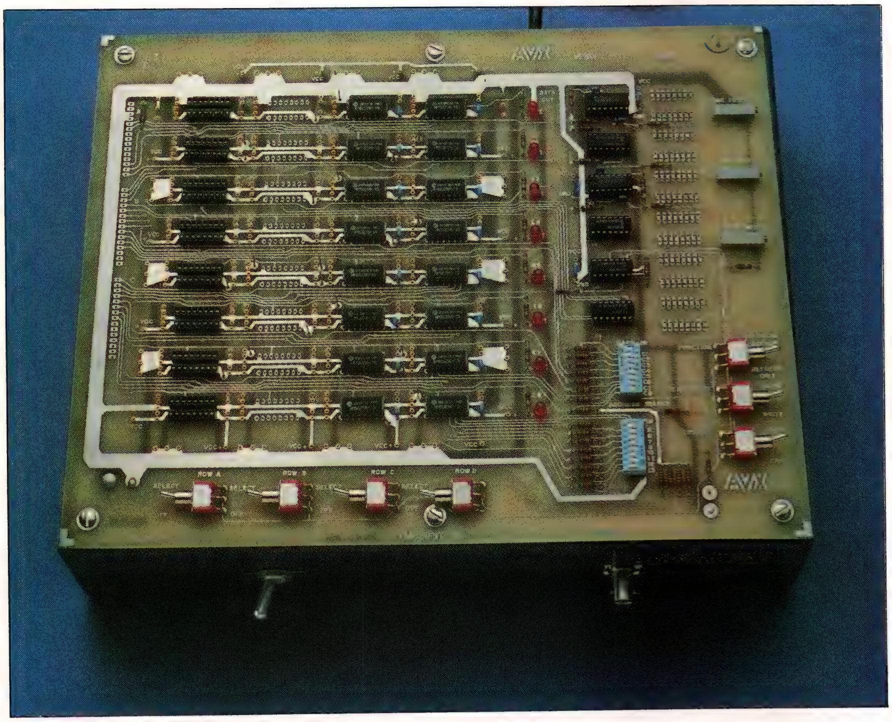

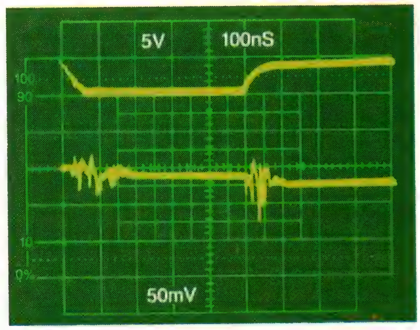

Fig. 2. Scope traces for refresh cycle on 256-K DRAM test board with 0.33-μfd AVX MLCs.

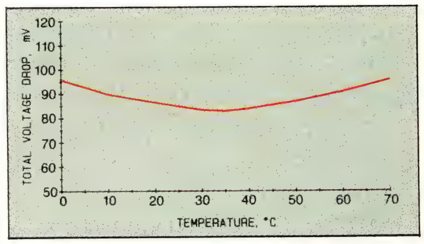

Fig. 3. Effect of temperature on 256-K DRAM decoupling with 0.33-μfd AVX MLCs (Z5U).

MLC Decoupling of 256-K Dynamic RAMs

A dynamic RAM's sensitivity to decoupling-induced "soft-errors" (random loss of one or more bits of memory) increases dramatically with higher speeds, higher density, and an increased number of sense amplifiers. The new 256-K DRAM designs have large, instantaneous current demands which must be satisfied by a local current source.

That source is the decoupling capacitor directly adjacent to the RAM package. And the capacitor most often used for this application is a multilayer ceramic capacitor (MLC) because of its low series inductance, low series resistance, and high capacitance in a small size.

Test Results

Tests were conducted by AVX on a 256-K DRAM memory board to determine the noise level obtained with various values of MLC capacitors. Figure 1 compares the results obtained using 256-K DRAMs with those from similar board tests on 64-K DRAMs. As indicated, 0.33-μfd capacitors are required on the 256-K DRAM board to obtain a noise level equivalent to that obtained using 0.1-μfd capacitors on the 64-K DRAM board. Performance improvements on the 256-K DRAM

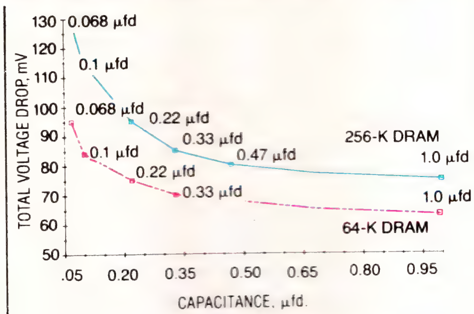

Fig. 1. Decoupling characteristics for 64-K and 256-K DRAMs with AVX MLC capacitors (including V-bump and V-droop).

test board leveled off between 0.33-μfd and 1.0-μfd, indicating that the preferred value for decoupling is about 0.33-μfd.

Figure 2 shows the scope traces obtained during refresh cycle on the 256-K DRAM test board with a 0.33-μfd AVX MLC. In all tests, the general decoupling scheme used was one MLC capacitor for each DRAM, with no board-level bulk capacitors.

Discussion

General-application ceramic formulations, such as Z5U, show considerable change in capacitance with temperature. However, this change has little affect on the total noise level for 256-K DRAM when the correct value is chosen. Thus, the 0.33-μfd value is high enough to meet the 256-K DRAM's current requirements over its full operating temperature range, as shown in Fig. 3.

For a complete technical paper describing these tests in detail, complete and return the coupon below.

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AVX Technology For The Times

CIRCLE NO 99

Program returns D/A input for new gain

Mario Bilac
General Electric Co, Plainville, CT

Fig 1 shows a digitally controlled gain circuit based on a multiplying D/A converter; the circuit implements the function $V_{OUT} = -V_{IN}/D$. In the function, D is the digital input interpreted as a fraction between 0 and 1. Determining by hand the optimum value for D to produce a desired gain can be cumbersome because many values may produce nearly the same gain.

Table 1 illustrates how a Fortran-77 routine determines D for the closest realizable approximation to the desired gain. The algorithm uses a trial-and-error process to solve for the coefficients A_N of the circuit's gain-transfer function, V_{OUT}/V_{IN} **(Fig 1).** Each A_N value is either 0 (bit off) or 1 (bit on). Although written as a design tool, the algorithm can also serve such real-time applications as adaptive gain control.

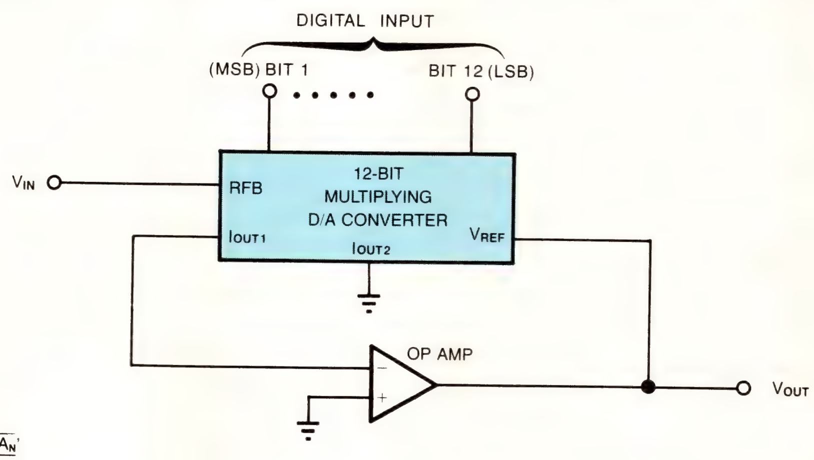
Given the desired gain and D/A-converter resolution, the algorithm steps are as follows:

1. Set the new gain equal to the desired gain.
2. Find i such that 2^i is greater than or equal to the new gain.
3. Compute the divisor of the transfer-function formula and store the result.
4. Compute the new gain by taking the reciprocal of the desired gain and subtracting the divisor value computed in step 3.
5. Determine if the new gain can be realized with the specified D/A converter's resolution. If the new gain is less than the converter's resolution, return to Step 2. Otherwise, all bits are determined.
6. If the desired gain is unity, set all bits to 1.

TABLE 1—ALGORITHM EXAMPLE*

STEP	FIRST PASS	SECOND PASS
1	NEW GAIN = 1.77	—
2	i = 1 (2^1)	i = 4 (2^4)
3	SUMBW = $\frac{1}{2}$	SUMBW = $\frac{1}{2} + \frac{1}{16}$ = 0.5625
4	NEW GAIN = $(\frac{1}{1.77} - \frac{1}{2})^{-1}$ NEW GAIN = 15.39	NEW GAIN = $(\frac{1}{1.77} - \text{SUMBW})^{-1}$ NEW GAIN = 404.57
5	G1 < 256 GO BACK TO STEP 2	G1 > 256 ALL BITS ARE DETERMINED
	D/A BITS: 1 2 3 4 5 6 7 8 DIGITAL INPUT: 0 1 0 1 0 0 0 0 ACTUAL GAIN = 1.7777 DESIRED GAIN = 1.77	

* THIS EXAMPLE ASSUMES AN 8-BIT D/A CONVERTER AND A DESIRED GAIN OF 1.77 V/V.



TRANSFER FUNCTION:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-1}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots + \frac{A_N}{2^N}},$$

WHERE THE COEFFICIENTS A_N, ASSUME A VALUE OF 1 FOR AN ON BIT, OR 0 FOR AN OFF BIT.

NOTES:
V_{REF} IS THE REFERENCE VOLTAGE INPUT.
RFB IS THE FEEDBACK-RESISTOR TERMINAL (NORMALLY USED WITH AN EXTERNAL OP AMP).
I_{OUT1} AND I_{OUT2} ARE RESISTIVE-DIVIDER OUTPUTS.

Fig 1—With this digitally controlled gain amplifier, *determining the optimum digital input for a desired gain is no straightforward task. The program in* ***Listing 1,*** *however, can do the job for you.*

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CIRCLE NO 101

Table 1 illustrates these steps with an example. **Listing 1** provides the Fortran-77 user-interface program Gainmain and the subroutine Gainsub, which implement the algorithm. Gainsub is followed by a program-output example that calculates the digital inputs corresponding to four gain values for a 12-bit D/A converter.

Fig 2 is a plot of gain error (percent difference between actual and desired gains) for a 12-bit D/A converter. The plot includes data at 1.1V/V intervals over 0.01 to 99V/V. The plot shows, for example, that you can obtain gain values of 10 and lower with less than 0.1% error. For lower error over this range, you must use a 14- or 16-bit D/A converter. **EDN**

To Vote For This Design, Circle No 750

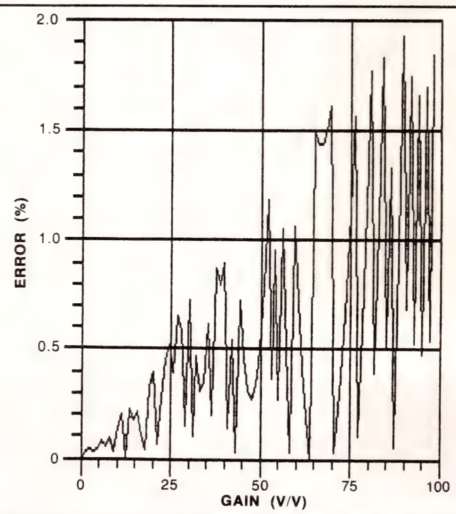


***Fig 2—This plot shows the percent error you can expect** between a desired gain and what you get using a 12-bit D/A converter and the 6-step algorithm. Data is plotted at 1.1V/V intervals.*

LISTING 1

```
         PROGRAM GAINMAIN

         DIMENSION Ix(12),Iy(12),Iz(12),Gainl(100)

c      Open an output file
           OPEN(UNIT=3,STATUS='NEW',CARRIAGECONTROL='LIST')

c      Get the desired gain

         Write(6,10)
10       Format(1x,' How many gains (up to 99 ) do you wish to determine?',$)
         Read(6,12) N
12       Format(i3)

         Do nl=1,N
          Write(6,11)nl
11        Format(1x,' Input the desired Gain',i2,' value ',$)
          Read (6,*)Gainl(nl)
         End Do

         Do nl=1,N
          gain=gainl(nl)
C      Clear all the bits in D/A
           Do k=1,12
                 Ix(k)=0
                 Iy(k)=0
                 Iz(k)=k
           end do

           CALL GAINSUB( Gain, Ix, Gl )

           WRITE(3,60) GAIN,Gl

           Do k=1,12
                 If (Ix(k).ne.0) Then
                  Iy(Ix(k))=1
                 end if
           end do

           Write(3,105) (Iz(k), k=1,12)
105        Format(1x,/,8x,'D/A Bits',10x,'(MSB)',12(1x,I2),1x,'(LSB)')

           Write(3,110) (Iy(k), k=1,12)
110        Format(8x,'Digital Input          ',12(1x,I2))

60       FORMAT(//,8X,'GAIN =',F10.5,5X,'ACTUAL GAIN=',F10.5)

         End do

         CLOSE(UNIT=3)
         END

          INCLUDE 'GAINSUB.FOR'
```

```
        Subroutine GAINSUB (Gain, Ix, Gl)

c  Gain = Desired gain, Ix(1) = matrix containing set bits
c  Gl = actual gain returned to the calling program.
        Dimension Ix(12),R(12)
c       Initialize variables
        SUMBW=0.0

C Step 1. Set new gain to equal desired gain
         Gl=Gain
c    The loop counter (L) is used to track the number of iterations
c    thru the complete set of steps.
        DO L=1,12
c Step 2. Find the 2's exponent for gain Gl using 12-Bit D/A
         DO i=1,12
                If ((2.0**Float(i)).GE.Gl) then
                 Ix(L)=i
                 go to 20
                End if
         End Do
 20      continue

c Step 3. Compute the transfer function divisor (SumBw).
         SumBw = SumBw +(1.0/(2.0**(float(Ix(L)))))

c Step 4. Compute reciprocal of the new gain
         Gl=ABS((1.0/Gain)- SumBw)
c       Test result - Can't divide by zero
         If (Gl.eq.0.0) go to 30
c       Set new gain
         Gl=1.0/Gl

c Step 5. Test if Gl is realizable with the 12 bit D/A
         If (Gl.gt.4096) go to 30

        End Do
 30     continue

c       Scale the original gain
        Gain=float(int(gain*10000.0))/10000.0

c Step 6. If gain is equal to 1.0 set all the bits of the D/A to a
c         logical '1'.
        If (gain.eq.1.0000) then
        Do k=1,12
         Ix(k)=k
        End Do
        End If

c       Compute the actual gain obtained by the circuit
         Gl=1.0/SumBw

        Return
        end
```

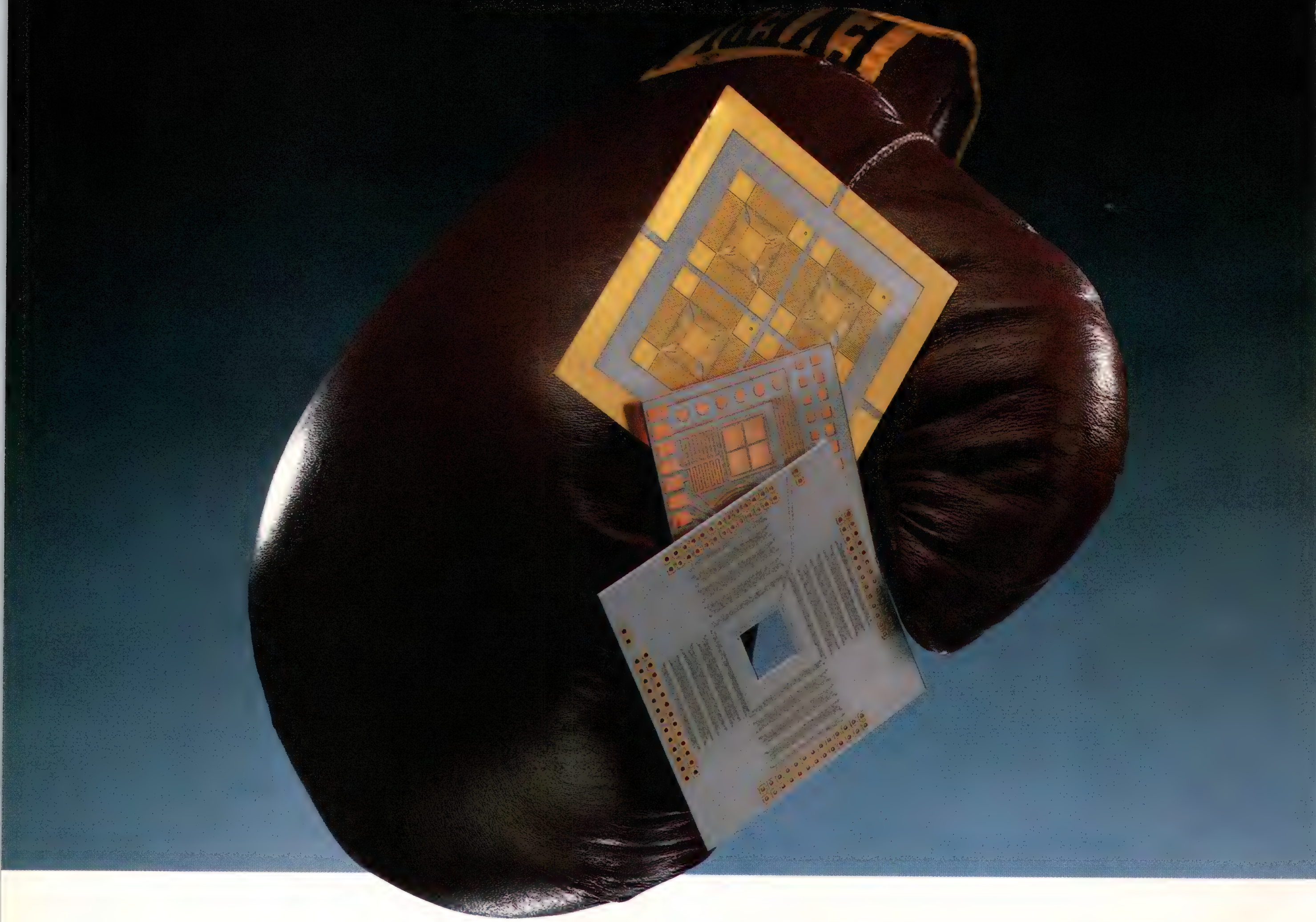
PROGRAM-OUTPUT EXAMPLE

```
1$ r gainmain
 How many gains (up to 99 ) do you wish to determine?4
 Input the desired Gain 1 value 32.567
 Input the desired Gain 2 value 12.459
 Input the desired Gain 3 value 6.789
 Input the desired Gain 4 value 3.2449


    GAIN =  32.56700      ACTUAL GAIN=  32.76800

    D/A Bits           (MSB)  1  2  3  4  5  6  7  8  9 10 11 12 (LSB)
    Digital Input             0  0  0  0  0  1  1  1  1  1  0  1

    GAIN =  12.45900      ACTUAL GAIN=  12.48780

    D/A Bits           (MSB)  1  2  3  4  5  6  7  8  9 10 11 12 (LSB)
    Digital Input             0  0  0  1  0  1  0  0  1  0  0  0

    GAIN =   6.78900      ACTUAL GAIN=   6.79270

    D/A Bits           (MSB)  1  2  3  4  5  6  7  8  9 10 11 12 (LSB)
    Digital Input             0  0  1  0  0  1  0  1  1  0  1  1

    GAIN =   3.24490      ACTUAL GAIN=   3.24564

    D/A Bits           (MSB)  1  2  3  4  5  6  7  8  9 10 11 12 (LSB)
    Digital Input             0  1  0  0  1  1  1  0  1  1  1  0
```

The

Challenge

to thick/thin film hybrid circuitry...



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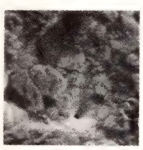
COMPARISON FACTOR	CERACLAD™	THICK FILM	THIN FILM
Conductor resistivity (Ohm-cm x 10^{-6})	1.7	15-60	1.7
Conductor thickness typical, (Inches x 10^{-3})	0.1-3.0	0.8	0.05
Circuit resolution (Conductors/inch/layer)	200	90	150
Typical circuit layers	2	1-3	1
Conductor adhesion (Lb/in²)	> 2000	1000	2000
Adhesion after heat aging (150 hr @ 175°C)	1800	850	1800
Wire bond strength (Grams)	13-15	8-11	13-15
Bond strength after aging (24 hr @ 160°C)	12-14	7-9	12-14

Copper thick film surface



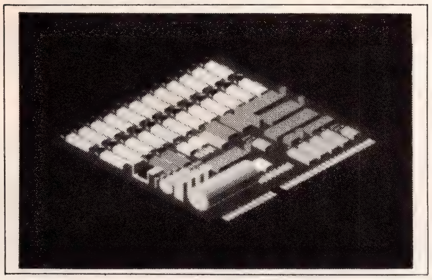
(magnified 1000x)

CERACLAD™ Copper surface

(magnified 1000x)

CERACLAD™ PRODUCTS GROUP
PCK TECHNOLOGY DIVISION
KOLLMORGEN CORPORATION
322 South Service Road,
Melville, NY 11747 (516) 454-4508

CIRCLE NO 102



PACKAGING DESIGN

An option to the T-Boards package combines pc-board-layout and electromechanical-design software. The combination lets you solve 3-D system interconnection and packaging problems that can occur when you design and test pc boards in their final packaging configurations. You can transfer 2-D circuit layouts into 3-D DDM (design, drafting, and manufacturing) mechanical-design files and check design interferences and analyze final designs. Using the DDM software, you can work with a picture of the design space and use manufacturing aids such as the Sheet Metal application package. The package runs on Apollo workstations. T-Boards starts at $77,000, including a color Apollo DN660 workstation; DDM software costs $50,000.

Calma Co, 501 Sycamore Dr, Milpitas, CA 95035. Phone (408) 434-4000.

Circle No 350

DRAFTING PROGRAM

Generic CADD is a 2-D design and drafting package that features multiple layers, multiple line types, user-definable fonts, rubberbanding line, video and digitizer menus, and component libraries. It requires an IBM PC with 256k bits of RAM, a color-graphics card, and a monitor. You can create drawings with a mouse or a digitizer. The editor provides lines, circles, arcs, ellipses, polygons, and components symbols. Two optional programs, Gen-Auto-Con and Gen-Dot-Plot, are available. Gen-Auto-Con converts AutoCAD drawing files to this company's CADD drawing files and vice versa; Gen-Dot-Plot drives 50 dot-matrix printers. Generic CADD, $99.95; Gen-Auto-Con and Gen-Dot-Plot, $24.95 each.

Generic Software Inc, 6 Lake Bellevue, Suite 203, Bellevue, WA 98005. Phone (206) 462-1944.

Circle No 351

GaAs-IC DESIGN

This GaAs-IC design kit, which runs on Daisy (Mountain View, CA) workstations, can help you develop Q-Chip GaAs MSI semicustom ICs. You can combine Daisy's schematic-capture and logic-simulation software with this company's logic macro library. Circuits can contain as many as 140 logic gates and 24 I/O ports; clock rates can range from 100 to 2000 MHz. $4000.

TriQuint Semiconductor Inc, Box 4935, Beaverton, OR 97075. Phone (503) 629-4227. TLX 4742021.

Circle No 352

FAULT-GRADING TOOLS

The IntelliTest/PFG probabilistic fault-grading software can analyze pc boards, as well as designs that you have created with a silicon compiler. The package provides vector development and fault grading for pc boards because it can accept behavioral functions. For silicon compilation and custom-VLSI designs, it can handle transistor models when gate-level descriptions aren't available. The package includes a library of behavioral models and transistor-level primitives. You can also add behavioral models to the library. The fault-grading package can interface to hardware modelers. An optional feature, Intellitest/DFTA, analyzes circuits from a topological point of view. This program searches for faults that are impossible or difficult to detect. DFTA provides a testability analysis of a circuit, interactive modification, and re-analysis and improvement reporting; it automatically suggests design modifications. It supports hierarchical macrolevel analysis and complex primitives (eg, Boolean functions, RAM, and ROM). PFG, from $5000; DFTA, from $2500.

Caedent Corp, 1901 N Union, Suite 102, Colorado Springs, CO 80909. Phone (303) 634-0722.

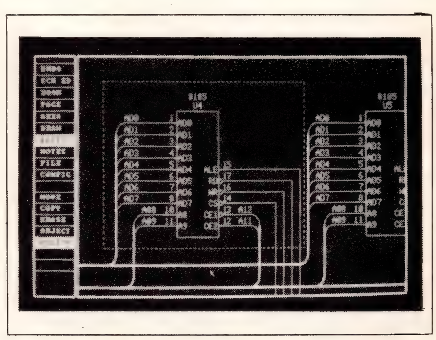
Circle No 353

LOGIC ACCELERATOR

The Mach 100 hardware accelerator simulates ICs and pc boards 500 times faster than does software running on a VAX 11/780, according to the manufacturer. The logic accelerator evaluates 250,000 events/sec and has a capacity for 32,000 modeling elements. It can accept behavioral models from a host workstation. Because the device understands the same command set as the simulation software that it accelerates, you don't need any training to use it. Occupying 20×10 in. of floor space, the unit can operate either as a dedicated hardware accelerator serving a single computer or as a shared peripheral that you can access via a LAN. $25,000 for logic simulation; $30,000 for logic and fault simulation.

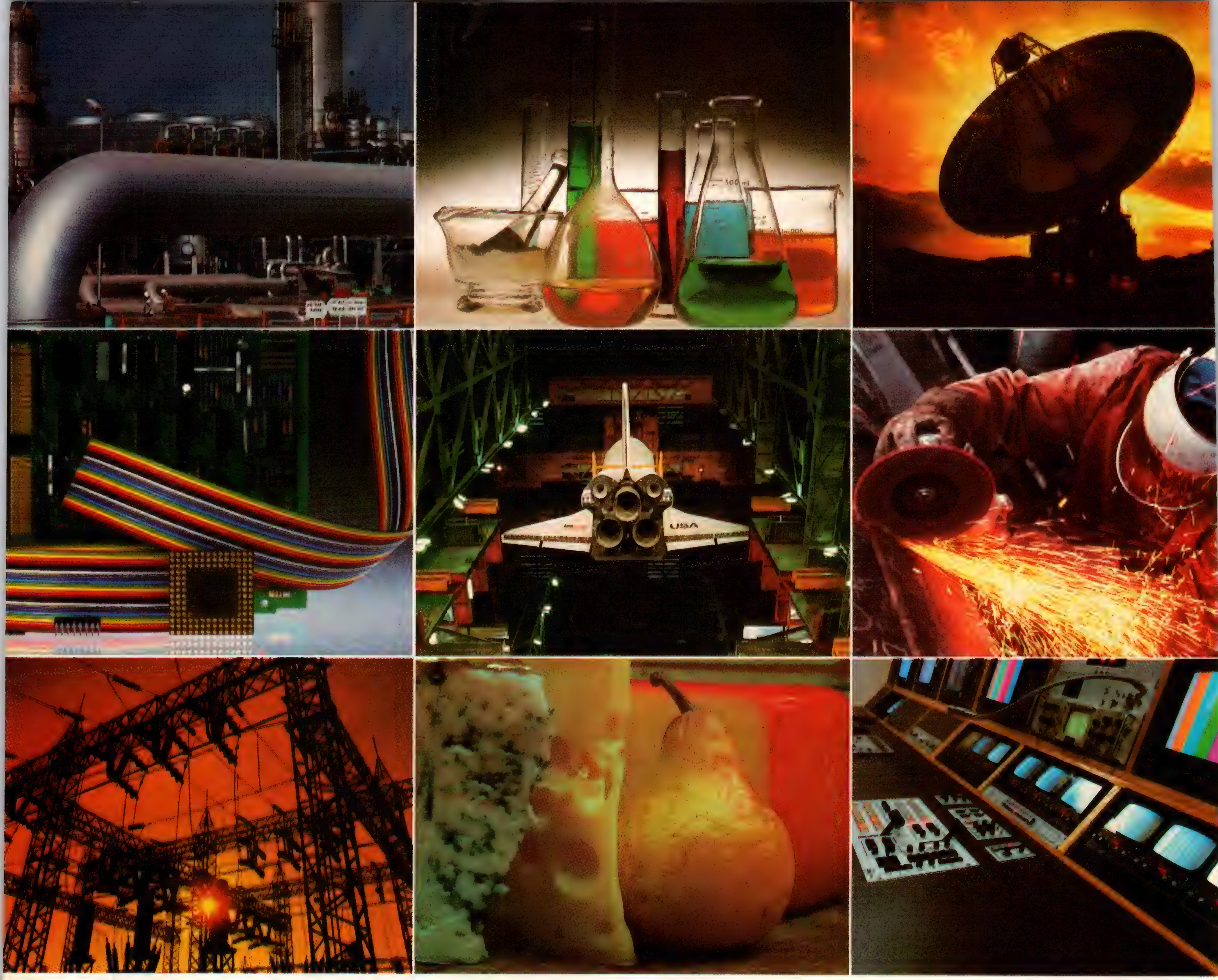
Silicon Solutions, 1380 Willow Rd, Menlo Park, CA 94025. Phone (415) 321-8574.

Circle No 354



SCHEMATIC CAPTURE

Schema, a schematic-capture program for the IBM PC, PC/XT, and PC/AT, lets you create drawings with a mouse. Because the manufacturer wrote this program in machine code, it delivers the fastest



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real-time screen graphics currently available for the PC. The program features postprocessors that extract net lists, wire lists, and bills of materials from schematics; the program also checks for design-rule violations. The design-rule checker locates and reports design errors such as floating inputs, nets that lack a driving source, nets that have multiple labels, and reference designators that you've used more than once. The package supports three graphics adapters: IBM standard color, IBM enhanced, and Hercules. It also supports most printers and plotters, including ones from Epson, Okidata, Hewlett-Packard, and Houston Instrument. $495.

Omation Inc, 1701 N Greenville Ave, Suite 809, Richardson, TX 75081. Phone (214) 231-5167.

Circle No 355

PC-BOARD DESIGN

Release 85.01 of the Scicards program features multilayer editing and routing, enlarged data limits, and automatic component placement. This version can lay out hybrid and surface-mount boards. It features a series of routers that automatically route as many as 32 board layers simultaneously. An automatic placement program can place analog boards, as well as digital and memory designs. The placement algorithm automatically prevents component-body and component-pin overlaps. The system can lay out boards that contain as many as 2500 components,

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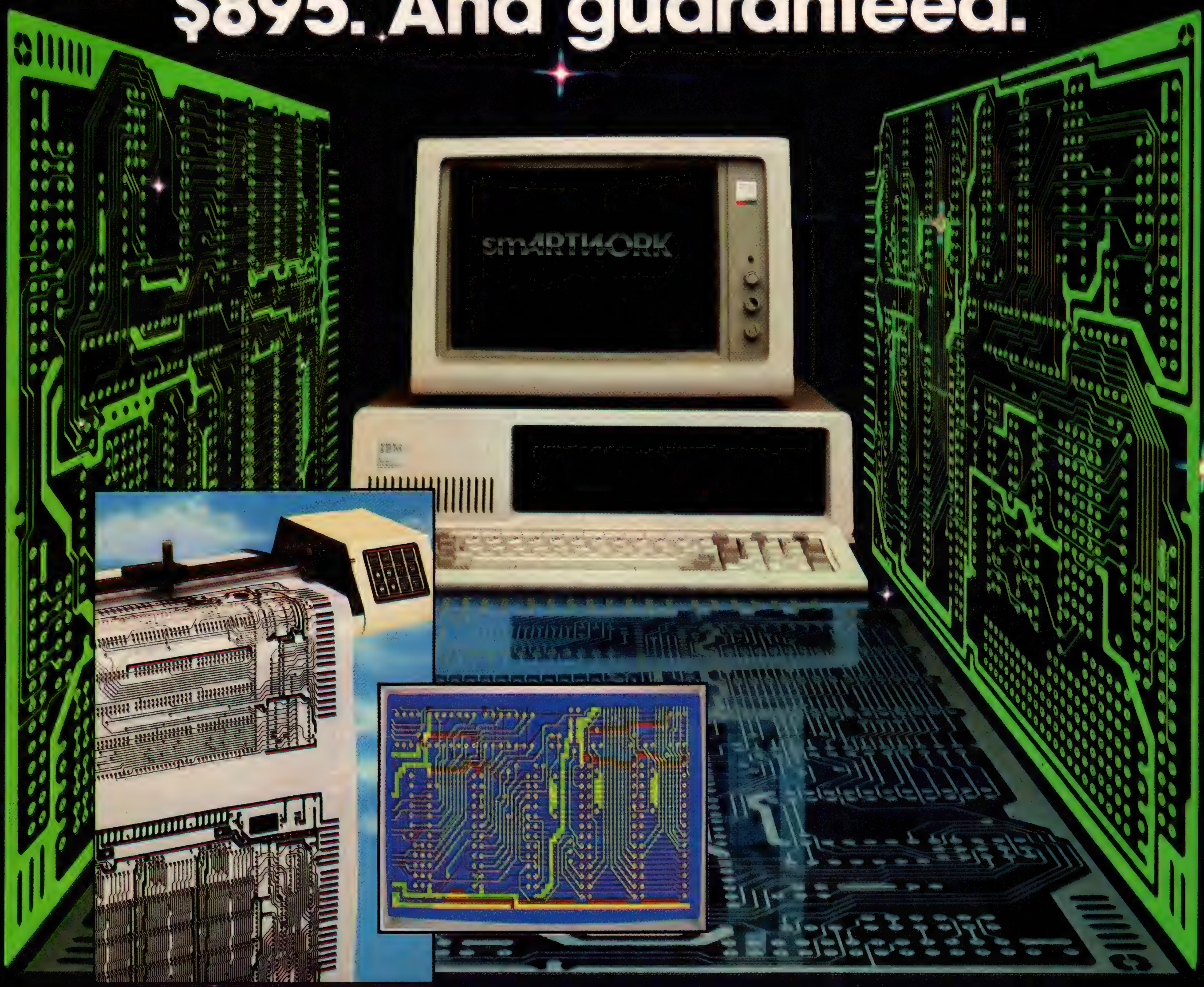

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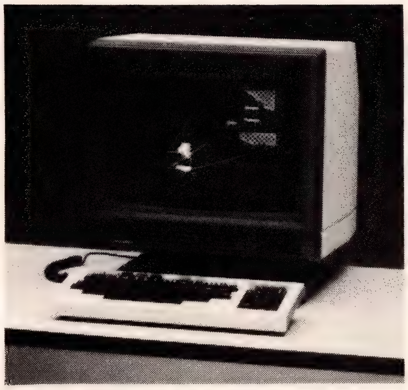
CIRCLE NO 104

250,000 pins, 10,000 nets, and 10,000 connections. $25,000 for a license for each station and $2000/month.

Scientific Calculations Inc, 7635 Main St, Fishers, NY 14453. Phone (716) 385-6790. TLX 978316.

Circle No 356



GRAPHICS TERMINAL

The CT 1024 Colorgraphic terminal features both 1024×1024 and 512×512 switchable bit-map displays in a modular 19-in. monitor. Under program control, you can operate the monitor in a 1024×768, 30-Hz, interlaced refresh mode or a 512×384, 60-Hz, noninterlaced refresh mode. It supports zoom, pan, blink, and eight or 16 simultaneous colors. Input devices include a light pen, a digitizing table, and a keyboard. $8495.

Chromatics Inc, 2588 Mountain Industrial Blvd, Tucker, GA 30084. Phone (404) 493-7000. TWX 810-766-8099.

Circle No 357

GRAPHICS TRANSFER

The Cadds 4X graphics-transfer package can move graphical information between the vendor's Personal Engineer or CDS 3000 workstations and the Cadds 4X CAD system. You can use this package to produce final documentation and to store these documents. The interface can pass libraries and schematics. By using the interface in conjunction with net-list-transfer and

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Device	Access Times	Max Current act	stby	Process
IMS1400 16K x 1	35,45,55	660	110	NMOS
IMS1420 4K x 4	45,55	605	165	NMOS
IMS1423 4K x 4	25,35,45	660	33 CMOS	CMOS
IMS1600 64K x 1	45,55,70	440	77 CMOS	CMOS
IMS1620 16K x 4	45,55,70	440	77 CMOS	CMOS

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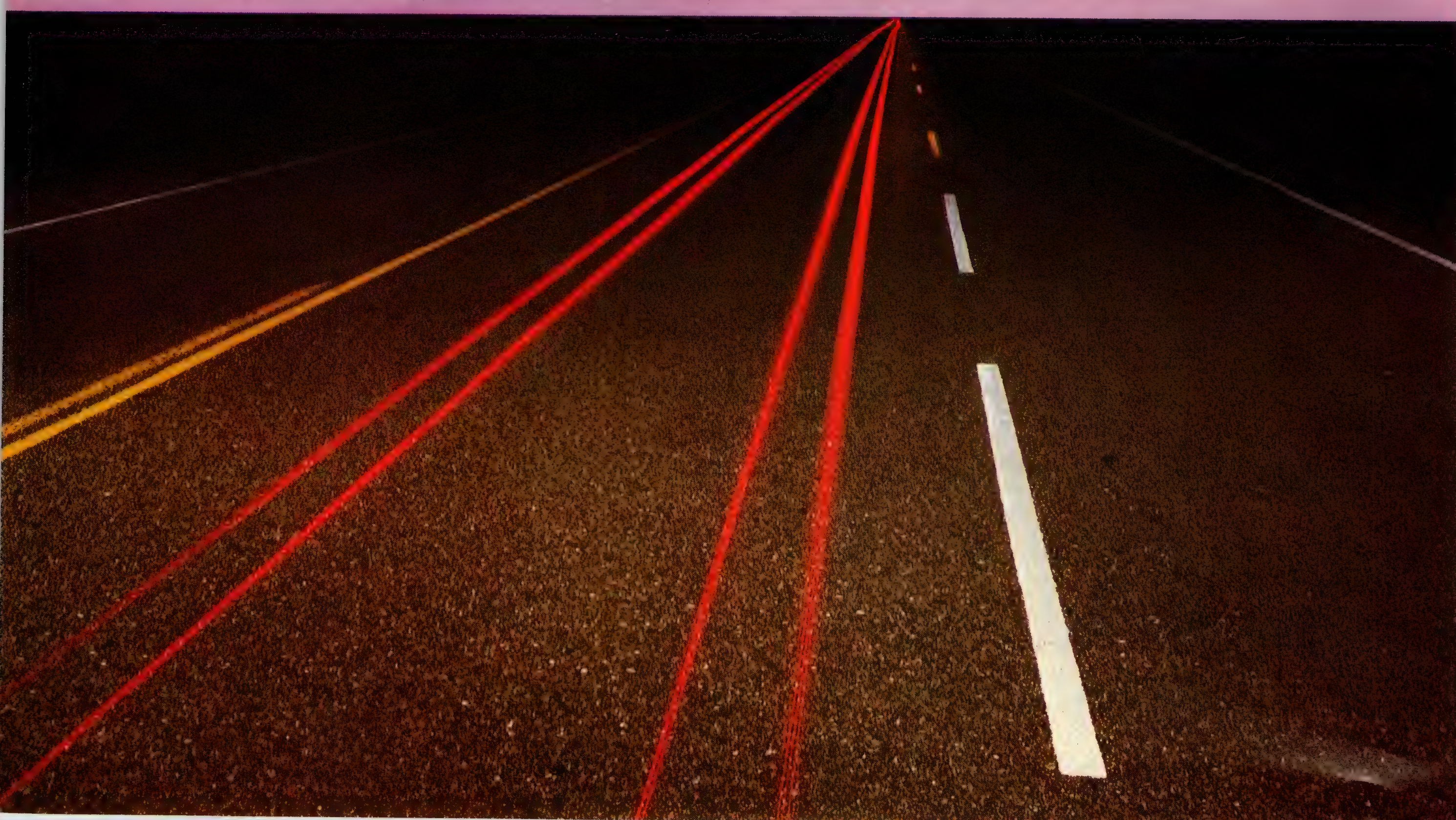


back-annotation utilities, you can make certain that your layouts reflect all revisions in your logic. $2700 for interface for Personal Engineer; $3900 for CDS 3000 interface.

Computervision Corp, 15 Crosby Dr, Bedford, MA 01730. Phone (617) 275-1800.

Circle No 358

PC-BOARD ANALYSIS

Wrapid, a layout package developed by Compion (Chapel Hill, NC), places components and checks for design-rule violations. It includes the vendor's databases of pc-board geometries, as well as communication software. The package can analyze the data from schematic drawings for such errors as missing devices and duplicate reference designators. The program runs on IBM PC-based FutureNet Dash workstations. $695 for the first diskette containing program and databases; $50 for additional databases. Delivery, 30 to 60 days ARO.

Augat Inc, Systems Div, Box 1037, Attleboro, MA 02703. Phone (617) 222-2202. TWX 710-391-0644.

Circle No 359

PC-BOARD LAYOUT

The V04 CAD system is a direct upgrade of the V03 and runs on DEC's PDP 11/73 computer. Its automatic, re-entrant router achieves 100% routing success in most cases, according to the manufacturer. The system handles component placement and routing of surface-mount devices (SMDs) automatically, and it also provides interactive tools for designing circuit boards containing SMDs. You can assign SMDs to both sides of a pc board. The system accelerates its graphics display with zoom and pan hardware; to zoom in on a designated area takes less than 1 sec. The graphics processor controls a 2048×2048-pixel display. The LSI 11/73 CPU and this company's


AEG

COMPUTER-AIDED ENGINEERING

RPR246 routing processor and a hardware accelerator operate in parallel. Upgrades of the V03, $20,000 to $60,000; 2-station V04 system, $179,980.

Calay Systems Inc, 2698 White Rd, Irvine, CA 92714. Phone (714) 863-1700. TLX 6711321.

Circle No 360

COLOR DISPLAY

The Workview Series now offers color displays. This enhancement accepts IBM-compatible color cards, including the IBM color-graphics adapter and the IBM enhanced graphics adapter. Four versions are available: an entry-level system, a digital-design system, an analog-design system, and an analog-and-digital design system. The entire series runs on IBM PCs and compatible computers. From $3500.

Viewlogic Systems Inc, 33 Boston Post Rd W, Marlboro, MA 01752. Phone (617) 480-0881.

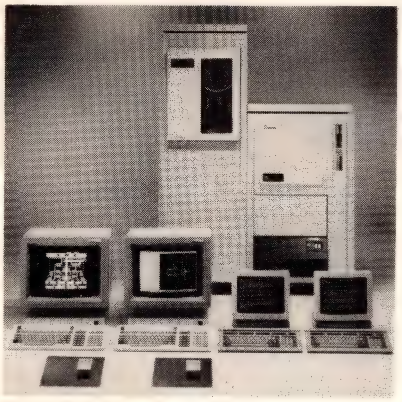
Circle No 361

SCHEMATIC EDITOR

This package for schematic capture and net-list extraction, Ski Cap, uses Autodesk's AutoCAD for its base software. You can connect components either by drawing lines between symbols or by associating the symbols via a common signal name. The library provides TTL and CMOS components. The net-list generation utility accepts single- or multiple-page schematic diagrams. The package also features a net-list linkage editor and postprocessor that creates a net list containing a consolidation of all nets from each page of a complete diagram. $1500; demonstration package, $50.

Micro Design Automation, 1260 Clearmont St NE, Bldg 5, Palm Bay, FL 32905. Phone (305) 725-8081.

Circle No 362



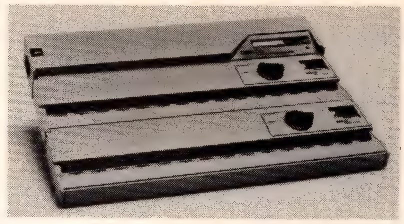
COMPUTERS

Microcomputers in the 5000 Family perform continuous calculations on large sets of data in real time. The five computers in the series come in table-top, pedestal, and cabinet configurations with as many as four 68020 CPUs. RTU, a real-time Unix-based operating system, offers compatibility with Unix System V and Berkeley 4.2 BSD. The triple-bus architecture includes a Multibus and an STD+Bus to increase data paths and add peripherals. The computers support Ethernet TCP/IP and X.25 communication protocols. Additional features include a floating-point arithmetic processor and a 2-way associative cache memory. These μCs offer data-acquisition rates to 1M samples/sec and computation speeds that range from 0.7 to 10 MIPS or as many as 13M flops. You can choose such graphics options as window managers and monitors with resolutions to 1152×910 pixels. $15,000 to $250,000.

Masscomp Corp, 1 Technology Park, Westford, MA 01886. Phone (617) 692-6200. TLX 704353.

Circle No 363

PROGRAMMER



The Series 1000 device programmer uses an 8-MHz 8188 CPU to program as many as 30 devices in parallel. You select programming commands, command options, and device names from scrolling menus on a 2-line LCD. The Scooptool lets you slide devices out of the manufacturer's tube directly into the programmer sockets. Socket isolation identifies single-device failures before they affect other sockets. Autocalibration monitors programming and supply voltages. The unit provides a safe power-down feature and self-diagnostics. It handles 24-, 28-, 32-, and 40-pin EPROMs, EEPROMs, one-time-programmable PROMs, and microcontrollers. The programmer comes in three configurations: The Duplicator pro-

grams only from a master device, the Downloader accepts data from either a master device or a remote computer, and the Virtual Memory Programmer uses an IBM PC's disk storage to extend the 1M-byte RAM. From $6500.

Data I/O Corp, 10525 Willows Rd NE, Redmond, WA 98073. Phone (206) 881-6444.

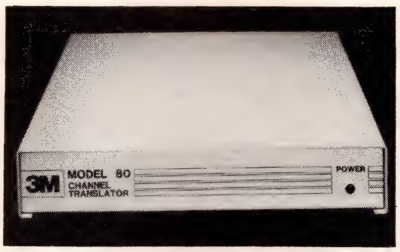
Circle No 364

HARD-DISK DRIVES

Internal Winchester disk drives in the FlexStor Series come in capacities of 25M to 80M bytes. Each is equipped with BackTrack, a software program that automatically backs up your files. Model 5525i, a 25M-byte half-height unit, costs $1195. Model 5535i offers 35M bytes of storage in a full-height chassis for $2395. The 50M-byte Model 5550i and the 80M-byte 5580i are full-height drives that cost $2595 and $3595, respectively. The Model 1000 full-length controller card costs $395.

Tallgrass Technologies Corp, 11100 W 82nd St, Overland Park, KS 66214. Phone (913) 492-6002. TLX 437121.

Circle No 365



TRANSLATOR

Providing uniform translation over five channels of operation, the Model 80 translator works with the manufacturer's LAN/I and LAN/PC to let you combine three networks on one broadband cable system. The unit requires no adjustments to use one or any combination of three channels. It provides network tolerance to large input signals that might contaminate a broadband network. Using the translator, the LAN will function properly when you apply one 18-dBmV input signal or two 15-dBmV signals. $590.

3M Interactive Systems, Dept IP85-32, 3920 Varsity Dr, Ann Arbor, MI 48104. Phone (612) 733-1186.

Circle No 366

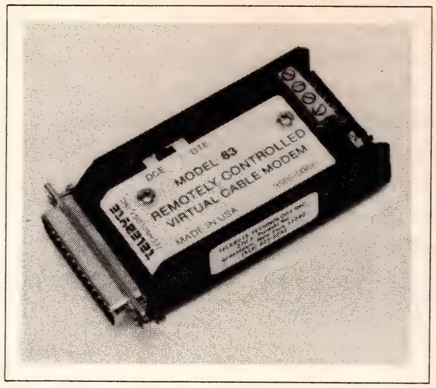
PC SPEECH

Your IBM or Apple PC can talk if you provide it with the Votalker, a pc-board and software product for speech synthesis. Featuring four preprogrammed voice patterns, the Votalker is based on the manufacturer's proprietary SC-02 speech chip. Software translators enable

your personal computer to speak with 32 inflections, sing in five octaves with 4096 pitch settings, and generate sound effects in 16 amplitudes. You can customize voices through two speaking modes and a voice filter; keyboard input isn't required for these switch-activated alterations. The Votalker's board plugs into a slot in your computer. The software includes a look-up table for proper pronunciation of difficult words. An external speaker jack is included. Votalker AP (Apple), $179; Votalker IB (IBM), $249.

Votrax Inc, 1394 Rankin St, Troy, MI 48083. Phone (800) 521-1350; in MI, (313) 588-0341.

Circle No 367

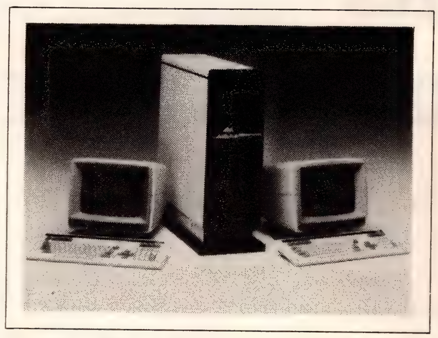


MODEM

The only operating power that the Model 83 modem requires is derived from your computer's I/O signals. This short-haul modem with bidirectional control and handshaking capability provides full-duplex transmission from dc to 19.2k bps through two twisted pairs. You control the modem remotely via its RS-232C connector or via a manually controlled switch. Error-free operation is ensured by the modem's differential baseband-signaling techniques and by common-mode signal rejection. As an option, you can substitute a modular RJ11 phone connector for the standard 4-wire interface. The modem measures 2.2×3.5×1 in. $68 (100).

Telebyte Technology Inc, 270 E Pulaski Rd, Greenlawn, NY 11740. Phone (516) 423-3232.

Circle No 368



68000 SYSTEM

Featuring a 10-MHz 68000 CPU, the Zebra 3750 computer includes 512k bytes of zero-wait-state RAM that you can expand to 2M bytes. The standard 64M-byte fixed Winchester drive has a 30-msec access time

and can support overlapped data searches in multiple disk configurations. The basic system also includes a ¼-in. streaming-tape drive, six asynchronous serial ports, one parallel printer port, and an internal uninterruptible battery-backup power supply. A control panel with a keylock switch prevents unauthorized use of the system; it also contains a reset switch, CPU status lights, power-on and battery-in-use indicators, and disk-drive activity indicators. $29,750.

General Automation Inc, 1045 S East St, Anaheim, CA 92803. Phone (714) 778-4800.

Circle No 369

DISK SYSTEM

Designed for use with an IBM Series 1 minicomputer, the Certainty 220 disk system provides 64.5M bytes of data storage on a 5¼-in. fixed disk. The disk drive stores

data on the nine data surfaces of its five disk platters. Average data-access time is 35 msec. Each disk features a dedicated head-landing area for locking down the data heads when you turn off power to the disk system, protecting stored data from damage when the drive isn't in use. The system's price includes a controller, cables, installation costs, and an operating manual. From $6500.

Control Data Corp, 2200 N Berkshire Lane, Minneapolis, MN 55441. Phone (612) 853-8096.

Circle No 370

MONITOR

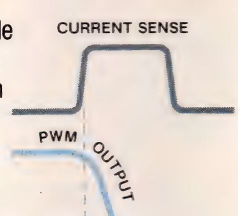
The IDT2000 green phosphor CRT lets you display one size-B drawing (11×17 in.) or two A-size drawings (8½×11 in.). The 19-in. monitor features 2048×1536-pixel resolution. Its graphic controller provides video frequencies to 200 MHz, a programmable screen format, and panning and scrolling functions for eight to 16 windows. The screen allows you to display large technical drawings or two A-size drawings simultaneously for comparison and correction. $14,900.

Image Peripherals Inc, 42 Nagog Park, Acton, MA 01720. Phone (617) 263-4005.

Circle No 371

UNIQUE SPEED

New Unitrode IC Can Drive Switchers To 1 MHz!

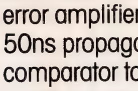


The barrier of slow logic control in switchmode power supplies has been broken!

Unitrode's UC3825 series is a new generation of high frequency pulse width modulators optimized for use through 1 MHz.

Propagation delay is minimized through the comparators and logic circuitry while the bandwidth and slew rate of the error amplifier are maximized. The result is an 8 MHz bandwidth error amplifier with a slew rate of 12V/μs and a 50ns propagation delay from PWM or current limit comparator to output.

Other features include start-up current less than 1.0mA, a trimmed bandgap reference, and all the protection circuitry you've come to expect from the leader in PWM's.



There's more! All this fast logic drives dual high speed totem pole outputs designed to source and sink 1.5 amp (pk) from highly capacitive loads such as power MOSFET gates.

Try the UC3825 for yourself. Fill in the coupon for a 1.5MHz Power Supply Evaluation Kit. Send a check for only $28, and you'll get a UC3825 and all the piece parts and literature to build a 50 Watt DC-DC converter. Or order the "UC3825 Kit" through our distributor, Hamilton-Avnet.

Unitrode Integrated Circuits
7 Continental Boulevard
Merrimack, New Hampshire 03054
Telephone: (603) 424-2410.

Please send me a 1.5MHz Power Supply Evaluation Kit so that I can try the UC3825 for myself. Enclosed is a check for $28. (Allow 6–8 weeks for factory orders.)

Name: ____________________

Company: ____________________

Street: ____________________

City: ____________ **State:** ______ **Zip:** ______

UNITRODE POWER AND CONTROL

CIRCLE NO 103

146-1477

The most precise, the most flexible control of power you can buy.

KEPCO POWER MANAGEMENT SYSTEMS™

KEPCO®

THE POWER SUPPLIER™

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THE POWER SUPPLIER™

KEPCO POWER MANAGEMENT SYSTEMS

consist of components that work perfectly together because they were *designed* to work together:

Kepco Power Manager™ and Kepco Digital Interfaces

The Kepco concept of Power Management, i.e., fast, accurate programming of voltage and current, was born more than three decades ago with the development — by Kepco — of the first programmable power supply. About a decade later, 20 years ago, we introduced the first programming interface. From their inception these components were designed to offer, both singly and as a system, a degree of control that was not only far beyond anything else available, but also far beyond the requirements of the time. Our programmable power supplies also included features (like "uncommitted amplifiers" and fast programming capabilities) for which there was then little demand, and for which many people could not even foresee a use.

Because Kepco has remained committed to the programming concept, today's Power Management Systems represent 30 years of improvement, refinement, and the incorporation of advancing technology. Today they offer a degree of control well beyond the capabilities of their predecessors — and are therefore still far ahead of anything else available. And so, while the requirements of the times have moved much beyond what they were in the 1960s, the Kepco Power Managers — and **only** the Kepco Power Managers — are well able to cope with them.

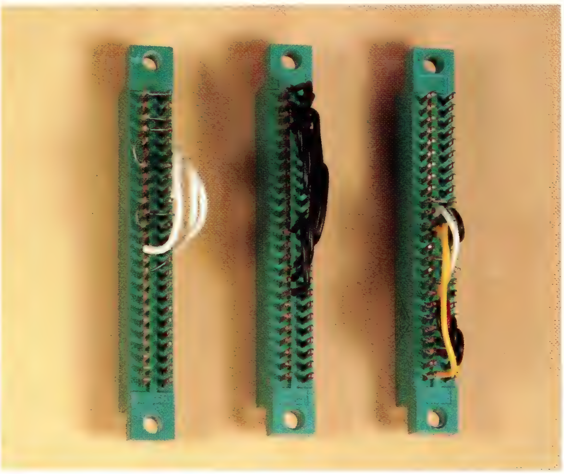
Kepco Power Managers

Power Managers are linear programmable power supplies designed to the operational power supply concept, patterned on the control possibilities inherent in a high gain, offset zeroed, operational amplifier. They have been especially designed for programming applications using either analog or digital control signals, and can scale a uniform 0-1V/0-10V (rangeable) or 0 to ±1V/0 to ±10V (bipolar) control signal into any desired output up to 1000 Volts and 1000 Watts, in some hundred different Volt/Ampere combinations. They give you maximum rated voltage and maximum rated current **simultaneously,** with full zeroing; and offset trim in both the voltage and current control channels. Additionally, the gain fixing resistors are a precision matched pair, so that power supplies may be substituted without recalibration.

The Kepco Power Managers are unique in two respects:

First, they are uncompromisingly linear — i.e., all stabilizing and controlling are done by the transistors constituting the series pass element.

Second, all nodes are accessible from the outside. Any element of a Power Manager's control assembly can be connected to any other through the external **"Rear Programming Connector,"** the simple plug shown, which mates with a 50-pin user port. It can be configured any way you want, and **re**configured any **time** you want, by merely removing some wires and adding others — inside the plug itself.



Rear Programming connector for a Kepco Power Manager configured for three different modes of operation.

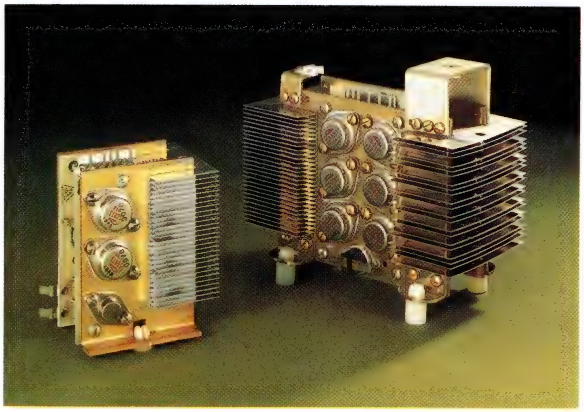
It is the Power Managers' uncompromising linearity that enables them to control voltage to 0.001% and current to 0.005%, from zero through their entire range; and to respond to programming step inputs in microseconds — also over their entire range. Only series pass control can give you such speed and accuracy, which derives from the fact that energy can be very quickly and precisely switched between a load and a lossy element.

But series pass control gives rise to considerable dissipation, because energy not immediately needed by the load is dissipated as heat. Most power supply manufacturers try to limit this dissipation with techniques like fold-back current limiting, tap switching, and switch mode operation of the control element. These tricks, however, greatly compromise speed, repeatability, and linearity in the control loop, or introduce such noise as to mask the small signal resolution of the system.

Kepco considers dissipation in the series-pass design not an unwanted by-product of an inefficient system, but a desirable form of energy storage. Energy can quickly be redirected from dissipator to load and vice versa. The system, when unencumbered by dissipation-limiting tricks, can turn the power to your load on and off in microseconds, and meter it in increments as small as 100 ppm.

The principal reason most manufacturers choose to inhibit dissipation is that they can't remove the heat that results from the dissipation fast enough to prevent dangerous temperature increases.

Kepco can. Our patented forced air heat sinks with integral fan remove heat so effectively that temperature rise is as little as 0.1°C/Watt. Thus while the Kepco Power Managers dissipate quite a lot, deliberately, they run cool, by design.



Kepco's patented heat sink,
with transistors mounted in TO-3 containers.

The Kepco ATE and BOP Power Managers employ a **variable reference/fixed gain** format. One advantage of this format is that it affords excellent protection to the power supplies' sensitive null junctions (the input point of the control amplifiers where the input signal joins the feedback signal) while controlling high voltage and high power, without the use of protective diodes and resistors. The leakage characteristics of these components, necessary in the conventional fixed reference/variable gain format, is another factor severely limiting the performance of most power supplies.

Another advantage of the variable reference/fixed gain format is that the roll-off characteristic is constant for all output settings, making the Power Managers stable over their entire range.

To provide the variable reference this format requires, separate op-amps are employed to convert a stable 6.2V temperature-compensated reference voltage into a linearly adjustable 0-10V control signal. This signal is linked to the main voltage amplifier (which has a voltage sensing feedback) and the current control amplifier (which has a current sensing feedback) through the Rear Programming Connector.

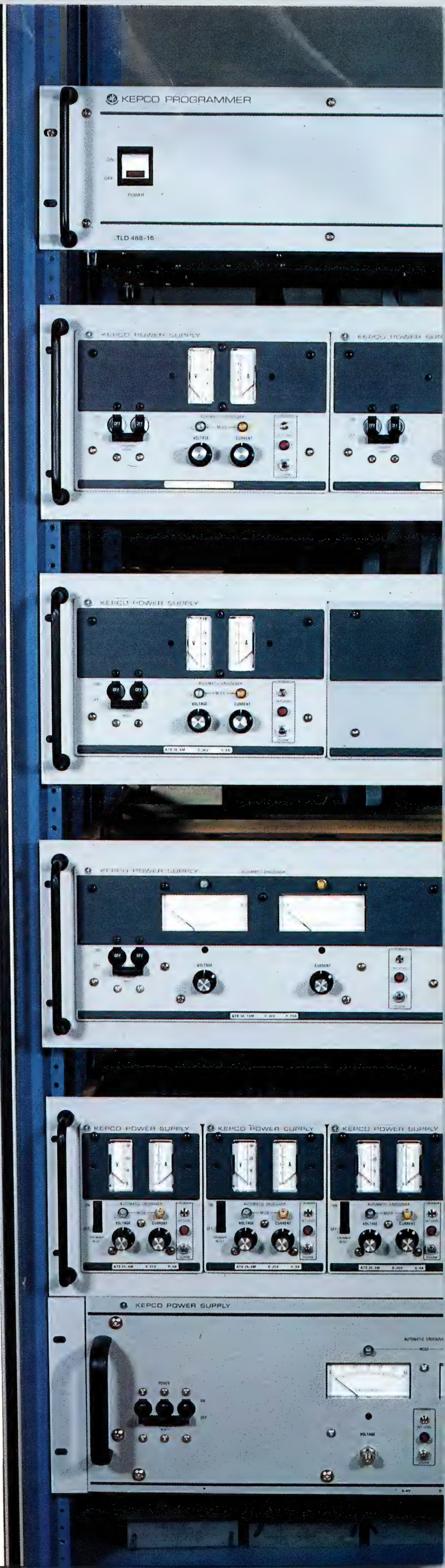
It is the accessibility of all their nodes through the Rear Programming Connector that gives Power Managers the flexibility no other power supplies can even approach.

Simply rewiring the external Rear Programming Connector* changes the very nature of a Power Manager. With one configuration it's a voltage supply, with another it's a current supply. By rewiring the plug, a single Power Manager can be a self-powered, oversized op amp, a servo amplifier, or a feedback stimulated current or voltage stabilizer. And that's only the beginning. Included in the Power Manager's control assembly are two "uncommitted" high gain amplifiers (which are also zeroable). As delivered, they are connected to nothing. But they can be connected, by simple rewiring of the Rear Program Connector, to give you voltage or current control with a two-terminal resistance, or with a high impedance variable voltage source. Or to scale, sum, invert, or integrate incoming signals. Or to do all sorts of exotic things, limited only by your imagination.

Interfacing with a Power Manager is also simply a matter of rewiring the Rear Program Connector. With the plug wired one way, the Power Manager is controlled by 10-turn front panel controls. By simply severing the link between the voltage control output and the voltage comparison amplifier (which is merely a matter of removing one wire from the plug), its voltage control channel can be programmed over its entire rated range by a zero to 10 Volt d-c signal. The current control channel can be similarly programmed. And both channels can be controlled simultaneously.

Since both the voltage and the current control amplifiers are zeroable and the sources of signal can be calibrated in terms of their full scale value, the only remaining variable is the linearity of the adjustment from zero to full scale. This is linearized by having at least 80 and typically 100 dB of closed loop feedback for a residual error in the range of 10-100 ppm

*Many of our customers prefer to keep a number of prewired plugs on hand, which makes changing from one mode of operation to another literally a matter of minutes.



— well within the resolution, for example, of the 12-bit digital-to-analog converters in Kepco's digital programming interfaces, which are guaranteed monotonic to within 1/2 LSB or 0.012%. In a Kepco Power Management System,

Power Management System assembled by Kepco, being computer-tested prior to shipment.

therefore, with a Kepco Digital Interface driving a Kepco Power Manager, the performance of the System is defined almost exclusively by the characteristics of the digital-to-analog converter in the interface.

The leads from the controlling source are connected to the Power Manager through that same external plug (or, in some models, through inputs provided on the front panel), and can come from an analog source, or from a digital source via a Kepco Digital Interface.

The Kepco Digital Interfaces

The digital interfaces were created to take full advantage of the Power Managers' precision and speed of response, by allowing them to be controlled by a computer or digital controller. The Interfaces translate 12-bit digital signals into a zero to 10V or zero to 1V variable d-c signal. Such programming is possible only because the Power Managers offer zeroing controls over the offset voltage and current on both the voltage and current channels. And, because they have 0.001% stabilization and noise levels significantly below that, 12-bit resolution is 0.024%; at 10:1 that becomes 0.0024%, well within the Power Managers' range.

Some Kepco Interfaces communicate with a computer via the IEEE bus, others via buses using bit parallel data transfer for faster transfer rates. Our interactive Model TLD 488 responds to commands in CIIL (Control Interface Intermediate Language) over the IEEE 488 bus, and also **listens** to responses from the Power Managers under its command, translates those responses into CIIL and passes them back to the computer. It can control up to 16 Power Managers at once, and not only can it single out a specific one to give a specific command to, but it knows which response came from which Power Manager.

The digital input and analog output of the Kepco Interfaces are optically isolated, so that their outputs may be used to control Power Managers which are also connected to other voltages or are grounded via their positive or negative output terminals.

This isolation is essential in automatic test systems, because the power supply for the digital I/O in most computers is grounded to the main frame, which is connected to the a-c power line. If not isolated, therefore, one of the Interface's output terminals would be connected to the computer's digital input common line, forming ground loops which could impair system operation and damage the computer and instruments.

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TLD 488-16. THE TALK AND LISTEN DIGITAL INTERFACE

When you command a power supply to go to a specific voltage or current setting, how do you (or more specifically, how does your controller) know whether the command has been obeyed?

If you're using a TLD 488-16, your Power Manager can talk back. It'll not only tell you **whether** it obeyed your command, but if it **didn't** it'll tell you **why**.

If, for example, you told it to go to 18 volts and it can't because that would cause an overload — it'll tell you.

Furthermore, the same TLD controlling **that** Power Manager can be controlling as many as 15 others at the same time.

Your controller communicates with the TLD via the IEEE-488 bus, and issues commands in CIIL at the level of protocol established for MATE (the Air Force's Modular Automatic Test Equipment system). It can tell the TLD to have a specific Power Manager go to a specific current setting with a specific voltage limit, or voltage setting with current limit.

If a Power Manager cannot obey a command, it responds with a flag which the TLD translates into CIIL and passes back to the controller as an "error message." These are the error messages it can send: crowbarred, overload, voltage comparison error, current comparison error, relay not closed or not open (referring to optional isolation relay TLR 25 or TLR 200), device not present *(i.e., no power supply was plugged into that particular input/output port),* no device selected, voltage out of range, and current out of range. The TLD also has a discrete fault *(or "status monitor")* line to report a catastrophic failure in itself or in the power supplies it is programming and monitoring.

The TLD itself is capable of detecting errors in the commands it receives *(e.g., a command that uses an unrecognizable op code, or is incomplete, or doesn't use the proper terminator),* and will inform the controller that it has made an error.

The TLD also translates the desired voltage or current settings into percentages of full scale, so that you can give your commands directly in Volts or Amps. What enables the TLD 488-16 to do this for 16 *different* power supplies at once is a special version of the Rear Programming Connector, called PCA. There's a PCA for every ATE model (BOP models use a plug-in card, as explained on the back page of this brochure). At turn-on, the TLD scans all the Power Managers under its command, and electronics in each PCA informs it of the voltage and power ratings of each of them. The TLD promptly memorizes this information, and uses it to calculate — for each Power Manager individually — what percentage of full scale a given voltage or current setting is.

The TLD consist of one single-board microcomputer which uses the 8088 CPU microprocessor, and as many as four plug-in analog boards (TL 488-4A, for controlling up to four ATEs, and TL 488-4B for controlling up to four BOPs), with which it communicates via the MULTIBUS* interface. The outputs of the boards are optically isolated from each other and from the digital interface circuit.

The unit is self-powered and has a very efficient cooling system.

**The MULTIBUS is a trademark of the Intel Corporation.*

Isolation Relays TLR 25 and TLR 200

Kepco offers two isolation relays which can be interposed between the power supply and the load in accordance with MATE system requirements: TLR 25, rated at 25 Amps, and TLR 200, rated at 200 Amps. They are operated by the TLD 488-16 through a separate, discrete interface and "I/O Isolation Relay Port", and respond to the CIIL commands "open" and "close". The address of each relay is set with a dip switch on the back of the relay.

These relays are mounted behind the power supply on Adapter ADR 1, which bolts on the back of full rack ATE or BOP models and holds one TLR 200; or on Adapter ADR 4, which holds four TLR 25s and bolts to the back of a special 7"-high rack drawer called RA-41.

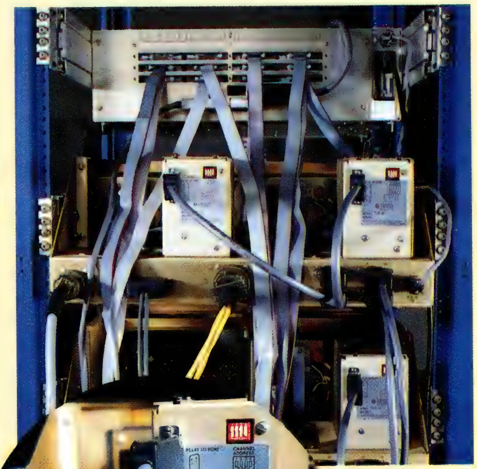
Isolation relays

MODEL	AMPS
TLR 25	25
TLR 200	200

Relay adapters

MODEL	BOLTS TO . . .	HOLDS . . .
ADR 1	Back of full rack ATE or BOP	1 TLR 200
ADR 4	Special 7"-high rack drawer, RA-41	4 TLR 25s

Isolation relays installed in rear of Power Management System.



Isolation relay TLR 25

Isolation relay TLR 200

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SERIES ATE. THE FAST AND SLOW POWER MANAGERS

These Power Managers are equipped with large output and feedback capacitors which can easily be connected or disconnected by the user.

When they're connected, these capacitors provide the filtering and energy storage required for varying load current. That's the "slow" mode. Disconnecting them puts the ATE into its "fast" mode of operation — increasing its bandwidth about a thousand times — so it can deliver constant current across a rapidly changing load voltage, or follow high speed voltage or current programming. In the fast mode, the 6-volt ATEs' programming time constant (their response to a programming step input) is 3 μsec.

Another important feature of the ATE Power Managers is their programmable overvoltage crowbar which can be manually set, be programmed, or track the signal controlling the output voltage.

QUARTER RACK 50W

MODEL	VOLTS	AMPS	MODEL	VOLTS	AMPS
ATE 6-5M	0-6	0-5	ATE 55-1M	0-55	0.1
ATE 15-3M	0-15	0-3	ATE 75-0.7M	0-75	0-0.7
ATE 25-2M	0-25	0-2	ATE 100-0.5M	0-100	0-0.5
ATE 36-1.5M	0-36	0-1.5	ATE 150-0.3M	0-150	0-0.3

QUARTER RACK 100W

MODEL	VOLTS	AMPS	MODEL	VOLTS	AMPS
ATE 6-10M	0-6	0-10	ATE 55-2M	0-55	0-2
ATE 15-6M	0-15	0-6	ATE 75-1.5M	0-75	0-1.5
ATE 25-4M	0-25	0-4	ATE 100-1M	0-100	0-1
ATE 36-3M	0-36	0-3	ATE 150-0.7M	0-150	0-0.7

HALF RACK 250W

MODEL	VOLTS	AMPS
ATE 6-25M	0-6	0-25
ATE 15-15M	0-15	0-15
ATE 25-10M	0-25	0-10
ATE 36-8M	0-36	0-8
ATE 55-5M	0-55	0-5

MODEL	VOLTS	AMPS
ATE 75-3M	0-75	0-3
ATE 100-2.5M	0-100	0-2.5
ATE 150-1.5M	0-150	0-1.5
ATE 325-0.8M	0-325	0-0.8

THREE-QUARTER RACK 500W

MODEL	VOLTS	AMPS	MODEL	VOLTS	AMPS
ATE 6-50M	0-6	0-50	ATE 55-10M	0-55	0-10
ATE 15-25M	0-15	0-25	ATE 75-8M	0-75	0-8
ATE 25-20M	0-25	0-20	ATE 100-5M	0-100	0-5
ATE 36-16M	0-36	0-15	ATE 150-3.5M	0-150	0-3.5

FULL RACK 1000W

MODEL	VOLTS	AMPS	MODEL	VOLTS	AMPS
ATE 6-100M	0-6	0-100	ATE 55-20M	0-55	0-20
ATE 15-50M	0-15	0-50	ATE 75-15M	0-75	0-15
ATE 25-40M	0-25	0-40	ATE 100-10M	0-100	0-10
ATE 36-30M	0-36	0-30	ATE 150-7M	0-150	0-7

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SERIES BOP. THE PLUS AND MINUS, SOURCE AND SINK POWER MANAGERS

Model BOP 100-4M

BOP stands for "Bipolar Operational Power Supply," which means that their output can be made to vary, linearly through zero, from plus to minus with respect to common, **through their entire voltage and current ranges.** They can produce a stable d-c voltage in the face of fluctuating current, or a stable current against fluctuating voltage, at any setting from 100% negative to 100% positive. Or they can follow complex programs which dance rapidly above zero, below zero, or above **and** below zero.

"Bipolar" also means that the BOP can absorb 100% of its rated voltage or current when its voltage polarity and current direction are out of phase, or when its load suddenly turns around and becomes a source.

Thus the BOP operates in all four quadrants of the Source-Sink plot. It is bounded in all four quadrants by four fully adjustable, programmable boundary limits.

The BOPs are also unique in that their digital-to-analog converter is a simple plug-in card that can be installed either at the factory when you buy it, or in the field later on. If desired, of course, the BOP will work perfectly with our stand-alone SN or TLD interfaces.

100 WATT

MODEL	d-c OUTPUT RANGE E_o max.	I_o max.
BOP 50-2M	± 50V	± 2A
BOP 100-1M	±100V	± 1A

200 WATT

MODEL	d-c OUTPUT RANGE E_o max.	I_o max.
BOP 20-10M	± 20V	±10A
BOP 36-6M	± 36V	± 6A
BOP 50-4M	± 50V	± 4A
BOP 72-3M	± 72V	± 3A
BOP 100-2M	±100V	± 2A

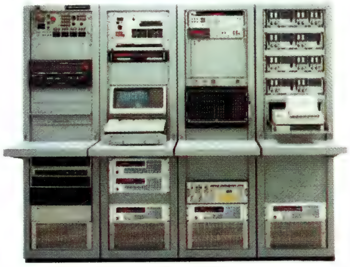
400 WATT

MODEL	d-c OUTPUT RANGE E_o max.	I_o max.
BOP 20-20M	± 20V	±20A
BOP 36-12M	± 36V	±12A
BOP 50-8M	± 50V	± 8A
BOP 72-6M	± 72V	± 6A
BOP 100-4M	±100V	± 4A

KEPCO POWER MANAGEMENT SYSTEMS AT WORK

The Power Management System shown at the right, consisting of a TLD 488-16 controlling five quarter-rack, three half-rack, one three-quarter rack, and one full rack ATE Power Manager, was put together, tested, and delivered as a unit by Kepco. Frequently, however, as in the three examples shown below, the Power Managers and Digital Interfaces are delivered as discrete components to the customer who integrates them into his own system.

Grumman uses one SNR 488-8 interface programming 11 ATEs in their CAT™ series automatic test systems.



The Harris Corporation uses one single channel SN 488-121 and four dual channel SN 488-122 interfaces programming 10 ATEs in their AN/USM-484 Hybrid Test System.

Honeywell uses one SNR 488-8 interface programming varying numbers of ATEs in their AEWTS and ETS Test Sets.

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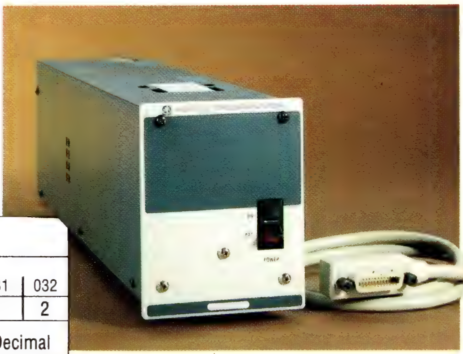
SERIES SN. STAND-ALONE DIGITAL INTERFACES FOR SINGLE OR MULTIPLE CHANNEL OPERATION

SN 488 is used with the IEEE-488 bus, and is available with one channel or with two isolated channels. If you buy the single channel model and later on find you need a second channel, you can buy a field-installable add-on channel. Output is 0 to ±10V or 0 to ±1V, selectable. SN 500 is the same as SN 488, except that it's intended for buses using bit-parallel data transfer.



	SINGLE AND DUAL CHANNEL PROGRAMMERS, ¼-RACK SIZE							
	SN488-				SN500-			
MODEL	121	122	031	032	121	122	031	032
NUMBER OF CHANNELS	1	2	1	2	1	2	1	2
INPUT DATA CODING FORMAT	Hex		Decimal		Hex		Decimal	
RESOLUTION	12 Bit		3 Digit		12 Bit		3 Digit	

SNR Housings

MODEL	HOLDS
SNR 488-4	4 Cards
SNR 488-8	8 Cards

Interface cards

MODEL	DATA FORMAT	RESOLUTION
SN 488-B	Hex	12-bit binary
SN 488-D	Decimal	3-digit BCD

SNR 488-4 and SNR 488-8 are card cages into which you can plug four to eight dual channel programming cards SN 488-B and/or SN 488-D. Each card, when installed, is isolated from the others, and contains two independently addressable (*but electrically common*) channels. All the cards use the same IEEE bus. The card cages contain an IEEE connector, an address select switch, a handshake card, a manual keyboard input connector, and local bus distribution for four to eight card sockets.

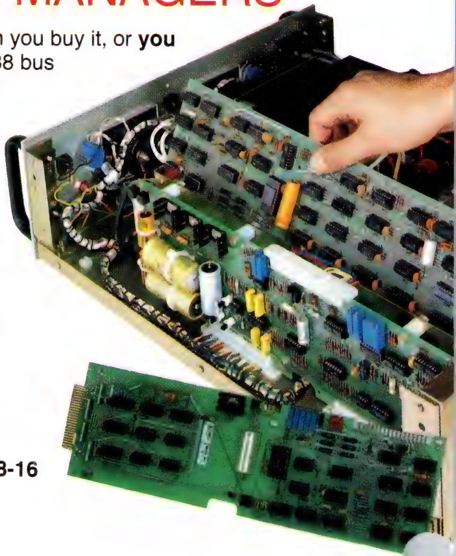
The input of the SN 488-B is coded in 12-bit hexadecimal; the input of the SN 488-D is coded in 3-digit BCD. The output of both is 0 to ±10V or 0 to ±1V, selectable.

SERIES BIT. INTERNAL DIGITAL INTERFACES FOR SERIES BOP POWER MANAGERS

These are the cards that either **we** plug into your BOP when you buy it, or **you** plug in later on, to provide an interface with either the IEEE-488 bus or a parallel data bus. They are dual channel, and can control voltage while limiting current, or control current while limiting voltage. Output is 0 to ±10V or 0 to ±1V, selectable.

			RESOLUTION		
SUFFIX(1)	MODEL(2)	DATA FORMAT	Principal Channel	Limit Channel	INPUT
—488-B	BIT 488-B	ASCII/Hex	12 Bits (binary)	8 Bits (binary)	For IEEE-488 (GPIB) bus
—488-D	BIT 488-D	ASCII/Decimal	3-Digit (BCD)	2-Digit (BCD)	For IEEE-488 (GPIB) bus
—500-B	BIT 500-B	Hexadecimal	12 Bits (binary)	8 Bits (binary)	For parallel data transfer bus
—500-D	BIT 500-D	Decimal	3-Digit (BCD)	2-Digit (BCD)	For parallel data transfer bus

(1) Add to model No. of the BOP to specify a factory-installed interface.
(2) Use this designation when ordering separately for field installation.



PCA X-3.
Internal Connector for BOP Power Managers, with TLD 488-16

This card plugs into the same slot as the BIT card, and is used to connect the BOP Power Managers with the TLD 488-16. It contains electronics that tells the TLD the voltage and current ratings of the BOP it's plugged into, so the TLD can translate voltage and current settings into percentages of full scale. The PCA X-3 contains voltage and current information for all the BOP models.

Data subject to change without notice

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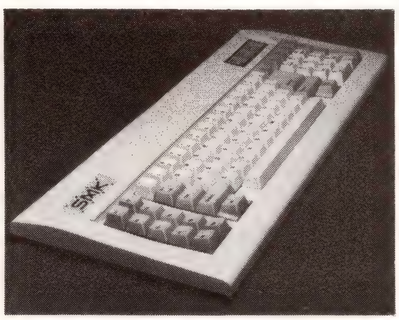
COLOR DISPLAYS

SCD (solid ceramic display) devices use PLZD (lanthanum-doped lead zirconate titanate) to produce 7-segment characters in more than 350 colors. DIP-socket mounted, these displays offer either light characters on a dark background or the reverse, in each of three viewing modes: reflective, transmissive, or transflective. They also offer typical ±80° viewing angles and −40 to +85°C operation. They require 190V typ drive signals and respond in 500 μsec max. Available high-voltage drivers include the 75552 from Texas Instruments. The displays meet MIL-STD-202. SCD706, $25 (1000). Delivery, six weeks ARO.

Motorola Inc, Ceramic Products Div, 4800 Alameda Blvd NE, Albuquerque, NM 87113. Phone (505) 822-8801. TLX 4999100.

Circle No 413

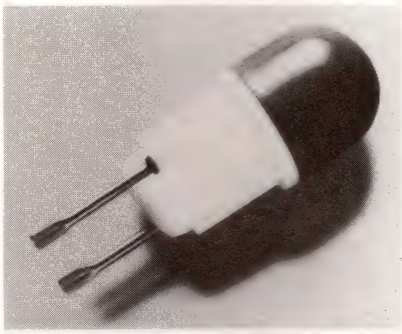


KEYBOARD

The KS 8300/AT keyboard is plug compatible with IBM PC and PC/XT computers but offers users of these machines the speed and convenience of the PC/AT's standard keyboard layout. IBM encoding is standard; ASCII and position encoding are available as options. The standard 19.2k-baud rate may be set as low as 1200 baud for special applications. A self-diagnostic routine is automatically initiated at power-up, and this company's IF key rollover circuit permits simultaneous activation of as many as eight keys. Keyboards are available either in a conductive-elastomer or a mechanical-switch configuration. $125.

Key Solutions, 10800 Normandale Blvd, Minneapolis, MN 55437. Phone (612) 884-7375.

Circle No 414



INDICATORS

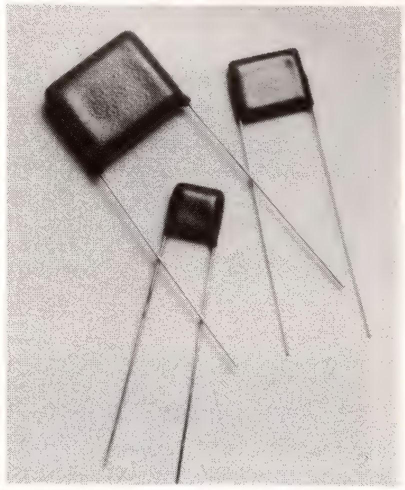
The Brite-Eyes BBE Series of subminiature indicators are available in red, white, yellow, green, and amber cap colors. You mount the indicator by inserting it in a 0.281-in. hole, and you replace the lamps from the front. Tools and mounting hardware are not required. Subminiature incandescent lamps are offered for the popular supply voltages, and a 117V neon lamp is also available. $0.74 (1000).

Shelley Associates, 14281 Chambers Rd, Tustin, CA 92680. Phone (714) 669-9850.

Circle No 415

CERAMIC CAPACITORS

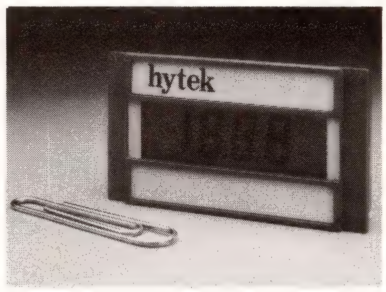
These high-voltage multilayer ceramic capacitors are fully tested for a corona level of less than 50 picocoulombs at the rated V_{rms} and less than 10 picocoulombs at 80% of the rated V_{rms}. This low corona level in the capacitor body increases the component's reliability, according to the manufacturer. Capacitors are



available with values from 10 pF to 0.22 μF, with voltage ratings from 500 to 3500 V_{rms}. $8 to $30 (100).

KD Components, 3016 S Orange Ave, Santa Ana, CA 92707. Phone (714) 545-7108.

Circle No 416

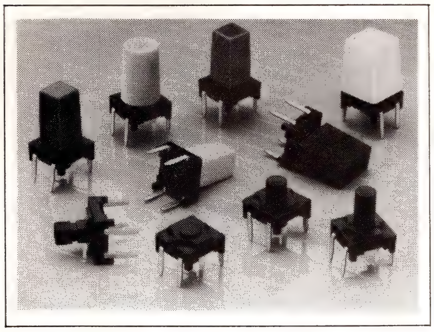


PANEL METER

The HY6300 is a 3.5-in. digital panel meter with 0.4-in.-high LCD digits and balanced differential analog inputs. It comes in a watertight compact package less than 0.5-in. deep and operates in harsh environments over 0 to 50°C. The device contains a custom hybrid circuit that can measure voltages from 100 μV to 200V and currents from 100 nA to 2A. It measures resistance from 1Ω to 20 MΩ. The meter is powered by a 9V battery requiring 12 mW of power or a 5V supply. $34.95.

Hytek Microsystems Inc, 980 University Ave, Los Gatos, CA 95030. Phone (408) 395-2300. TWX 910-597-5393.

Circle No 417

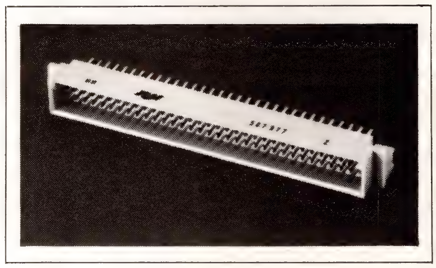


KEYSWITCHES

CDS-PR Series keyswitches are spst NO momentary-action switches that spec a contact rating of 50 mA at 20V dc. You can mount these keyswitches in a 0.1-in. pc-board layout grid. They are compatible with automatic soldering and cleaning processes. The units feature an operating range of −10 to +70°C. $0.15 (10,000).

Centralab Inc, 5855 N Glen Park Rd, Milwaukee, WI 53209. Phone (414) 228-7380.

Circle No 418

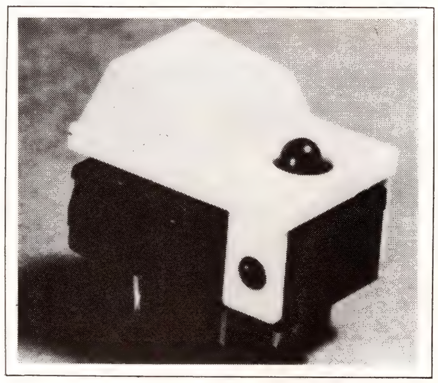


DIN CONNECTORS

The RNE Series standard and inverse DIN 41612 connectors feature selective loading of extended pins. The pins provide first-to-make, last-to-break ground contacts that protect sensitive CMOS circuitry from static discharge and high-voltage shock. The series is available with 32, 64, or 96 pins in either straight- or right-angle-mount styles. $0.04 per contact (100). Delivery, eight weeks ARO.

Robinson Nugent Inc, 800 E 8th St, New Albany, IN 47150. Phone (812) 945-0211.

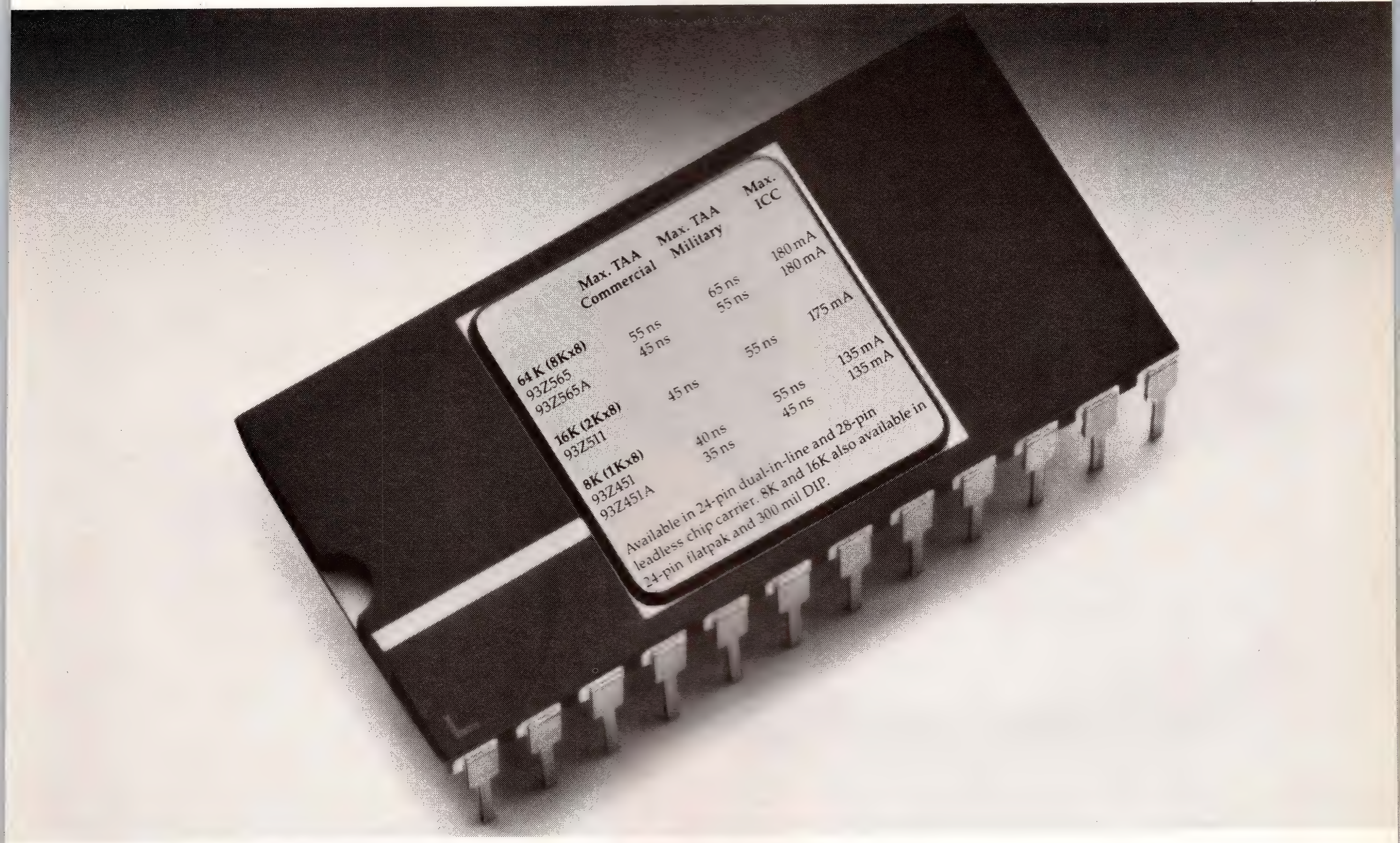
Circle No 419



MOMENTARY SWITCHES

You can use the SMG Series momentary key switches with dual-in-line packages. The manufacturer offers two button styles. You can select switches with or without LED illumination; red, green, and yellow LEDs are available. The switches use a reliable mechanical contact and have a service life exceeding

IF YOU WANT THE FASTEST 64K PROM, YOU'LL HAVE TO PAY A LITTLE LESS.



The Fairchild 93Z565A. One of the first 64K PROMs on the market and still the fastest. Giving you access time of 45 ns.

But that's not all.

Since we've been making them for over two years, we also know how to make them more cost-effective for your application. Which means you can confidently design with our 64K now and realize a lower cost-per-bit at the system level. And you'll find one 64K to be significantly more efficient than several 8K, 16K or 32K devices.

If you have an application requiring high speed at a lower density, we have a 16K PROM at 45 ns and an 8K PROM at 35 ns. Both in space-saving 300 mil DIPs.

It all adds up to the fastest PROM family ever built. PROMs that use Fairchild's Isoplanar-Z™ technology. With vertical fuse technology giving you one of the highest programming yields in the industry.

Our family of high-speed,

For more information, call The Fairchild Information Center at 1-800-554-4443 or write Fairchild Memory and High Speed Logic Division, P.O. Box 5000 MS 2C17, Puyallup, WA 98063-9701.

PROMs

FAIRCHILD

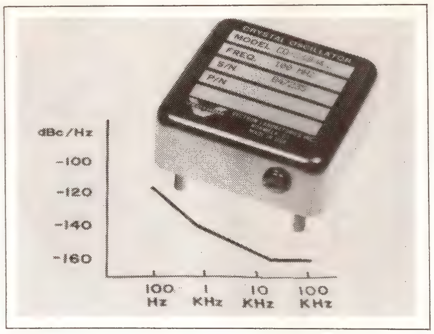
A Schlumberger Company

CIRCLE NO 163

1,000,000 cycles. The pushbutton is available in red, green, gray, blue, white, or black. Hot stamping is available for added flexibility. Unlighted version, $0.62; lighted version, $0.90 (1000).

Shelly Associates, 14281 Chambers Rd, Tustin, CA 92680. Phone (714) 669-9850.

Circle No 420

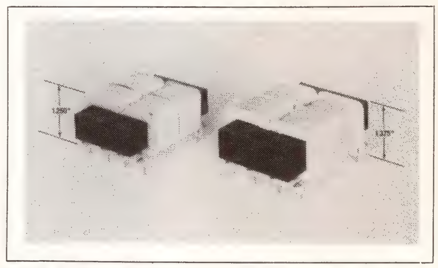


OSCILLATORS

The CO-233L2 Series of crystal oscillators offers a noise floor below −160 dBc/Hz for any frequency you specify in the range from 5 to 200 MHz. The oscillators have an aging rate of 2 ppm per year and are available with several stability options, ranging from ±3 ppm over the 0 to 50°C range to ±50 ppm over the −55 to +125°C range. Initial accuracy is ±10 ppm at 25°C, but a tuning option permits an accuracy setting within ±1 ppm. Output level is 7 dBm into 50Ω (13 dBm is available as an option). Each oscillator comes in a 2×2×0.75-in. case with a capacitively filtered input and an SMA output. $285. Delivery, 90 days ARO.

Vectron Laboratories Inc, 166 Glover Ave, Norwalk, CT 06850. Phone (203) 853-4433. TWX 710-468-3796.

Circle No 421



TRANSFORMERS

Low-profile, split-bobbin transformers in 24- and 48-VA ratings have been added to the company's Flathead Series. They include rugged, square-wire, plug-in pins capable of handling the devices' weight and amperage. Height above the pc board is 1.25 and 1.375 in. for the 24- and 48-VA units, respectively. Secondary output ratings for the 24-VA size range from 10V center tap at 2.4A to 28V at 850 mA (series-connected); the 48-VA size ranges from 10V center tap at 4.8A to 56V at 425 mA (series-connected). 24-VA version, $7, 48-VA, $9.

Signal Transformer Co, 500 Bayview Ave, Inwood, NY 11696. Phone (516) 239-5777.

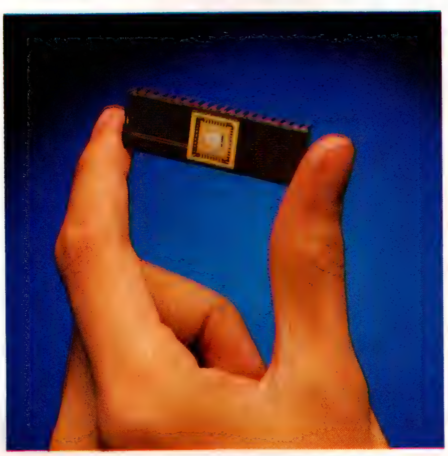
Circle No 422

If you're having a whale of a problem getting your system down to size...

CTD holds the solution.

At CTD, we offer total system integration with our TM6000 Silicon Gate CMOS Analog/Digital Semi-Custom Array, plus CMOS Digital Gate Array and Thick Film Hybrids.

Our Macrocells Library, available on Daisy CAE workstation and in hardware kit parts, include D/A, A/D converters, VCO, switched capacitor filters, and many



more. Call or write today to order our comprehensive TM6000 Design Manual at US$70.

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CIRCLE NO 121

HEAT SINKS

Models 6214 and 6216 provide maximum thermal performance using a minimum of pc-board space. They provide better heat transfer from the TO-3 transistor because of thick metal construction and tall sides with more surface area to dissipate heat. The wrap-around design results in less wasted material in manufacturing to keep the cost low. Model 6214 measures 1¾-in. tall and has a thermal resistance of 4.7°C/W at 75°C mounting surface temperature rise. Model 6216 is 2¼-in. tall and has 4°C/W thermal resistance. A choice of solderable studs or nuts provides wave soldering compatibility. 6214, $0.44; 6216, $0.49 (1000).

Thermalloy, Inc, Box 810839, 2021 W Valley View Lane, Dallas, TX 75381. Phone (214) 243-4321.

Circle No 423

TRANSMITTER

The Model FSK-T miniature thick-film transmitter operates from 44 to 63 MHz and has a center frequency of 57 MHz ±100 kHz. Modulation is phase-continuous frequency shift keying, with a deviation of 0.5 MHz ±2%. Data rates can be as high as 1.544M bps. Carrier second harmonic is attenuated by more than 60 dB. Output impedance is 75Ω, and VSWR equals 3:1 from 5 to 300 MHz. The transmitter comes in a 1.5×1.5-in. DIP. Less than $100.

Tektron Micro Electronics Inc, 7483-A Candlewood Rd, Linthicum Heights, MD 21090. Phone (301) 850-4200.

Circle No 424

CARD CONNECTORS

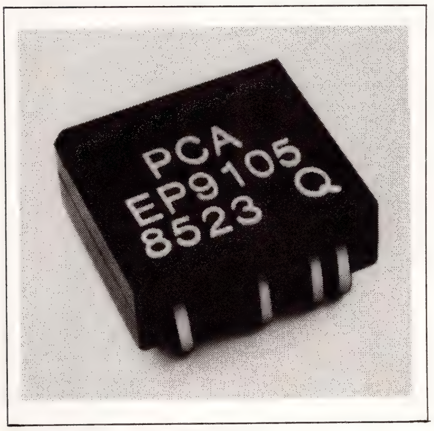
Offering 20 to 684 contacts, Series 9082 2-row, Series 9083 3-row, and Series 9084 4-row connectors have standard keying; the 3- and 4-row versions also come in no-guide-pin, single-guide-pin, or double-guide-pin variations. The 0.1-in. centerline, 0.025-in. square-post connector is made of high-temperature thermoplastic and is available in pc-board and wire-wrap straight posts and compliant-pin post terminations. The mating receptacle provides a 1.5-oz max insertion force

CIRCLE NO 122

and a normal force of 70g. Series 9082, $0.14 to $0.15 per line; 9083, $0.13 to $0.14; 9084, $0.12 to $0.13 (1000). Delivery, eight to 10 weeks ARO.

Elco Corp, Connector Div, Huntingdon Industrial Park, Huntingdon, PA 16652. Phone (814) 643-0700.

Circle No 425

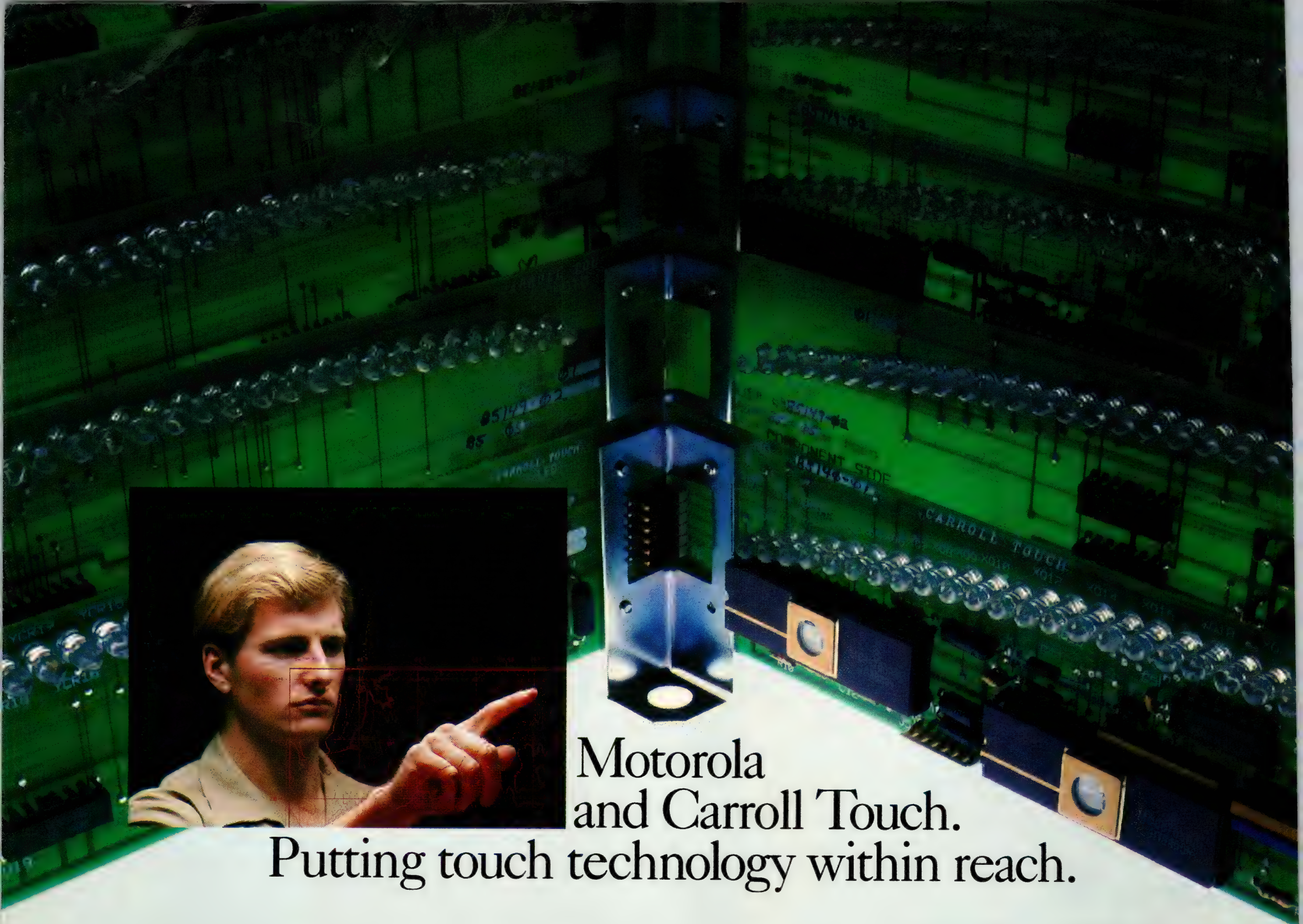


DELAY LINES

Units in the EP9100 Series of 5-tap delay lines conform to the proposed JEDEC 28-pin surface-mount-package specification. Total delay times of the 15 units range from 25 to 550 nsec ±5% or 2 nsec. Delay-line taps are equally spaced; the 250-nsec EP9114 has taps at 50, 100, 150, and 200 nsec. A Schottky TTL inverter buffers each delay-line input and the five output taps. The output buffers can drive a fan-out of 10 Schottky loads; maximum rise time is 4 nsec. The transfer-molded package is 0.450-in. square and has a mounted height of about 0.174 in. You can install them by vapor-phase or reflow soldering. The units use a 5V supply; supply current is 60 mA. Operating temperature is 0 to 70°C. $3.57. Delivery, six weeks ARO.

PCA Electronics, Inc. 16799 Schoenborn St, Sepulveda, CA 91343. Phone (818) 892-0761.

Circle No 426



Motorola and Carroll Touch. Putting touch technology within reach.

When Carroll Touch, Inc. decided to redesign its line of touch input products, it had two major goals. One was to reduce the number of parts by 50 percent. Which meant Carroll Touch™ could drastically cut its manufacturing costs. And lower its price in the market.

The second goal was to build in an abundance of flexibility in a base product. This would allow Carroll Touch to expedite orders for custom systems. As well as respond to rapid changes in its market.

Carroll Touch achieved both of these goals when it unveiled its first model of the Smart-Frame™ scanning infrared touch input system. And the key ingredient was Motorola's MC68705R3 microcomputer.

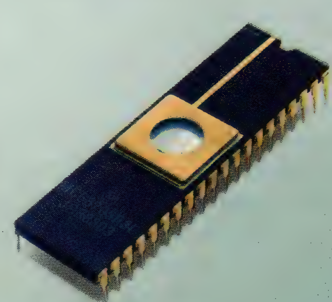
The MC68705R3 with its built-in EPROM gave the new Smart-Frame unprecedented flexibility. Special features could be added or changed by reprogramming Motorola's MCU instead of replacing it.

Because the MC68705R3 is a full-function microcomputer, most I/O support chips were eliminated. And many functions previously handled by task-specific hardware could now be handled by Motorola's MCU through software.

Motorola also satisfied the stringent requirements for reliability. Serviceability. And price. The MC68705R3 costs significantly less than its closest competitor. Yet its functionality and overall performance are significantly greater.

Fewer parts. More flexibility. Higher performance. The successful blending of two advanced technologies.

Together Motorola and Carroll Touch are putting touch technology within reach.



CIRCLE NO 124

Carroll Touch
a subsidiary of **AMP** Incorporated

MOTOROLA®

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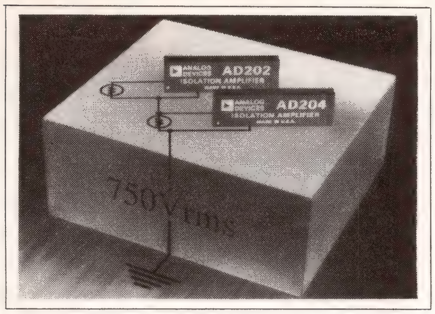


ISOLATION AMPS

The AD202 and AD204 use a solid-state transformer-isolation design, eliminating the need to buy a separate dc/dc converter. According to the manufacturer, the parts are the industry's lowest cost isolation amplifiers. Isolated power to floating-signal conditioners, front-end buffer amplifiers, or transducers is rated at ±7.5V at ±2 mA. The amplifiers feature minimum ±1000V peak (750V rms) common-mode isolation and ±0.05% maximum nonlinearity. Operating from a 15V supply, the AD202 suits multichannel applications, and the AD204 suits single-channel applications. Rated performance is over the 0 to 70°C range; however, the isolators also operate over −25 to +85°C. AD202, $28; AD204, $25 (100).

Analog Devices, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 329-4700. TWX 710-394-6577.

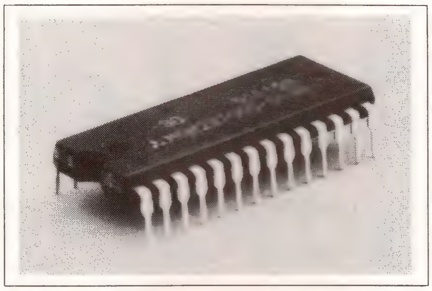
Circle No 372

FLOPPY-DISK IC

The FDC 9239 enhanced floppy-disk interface circuit incorporates a high-precision digital data separator, write-precompensation logic, and a programmable head-load timer. Using 2-μm n-well CMOS technology, the circuit provides the speed necessary to operate from a 16-MHz clock, which in turn is necessary to provide 16-bit resolution in the data-separator circuit. The IC breaks up incoming disk data into 16 discrete pieces and operates on those pieces individually, providing adjustment-free data separation for high-density floppy-disk drives, according to the supplier. It operates from a 5V supply and draws less than 20 mA typ. Depending on the version, you can choose from circuits that work with 3¼-, 5¼-, and 8-in. disk drives. You can also choose from 20-pin plastic or ceramic DIPs or cerdips. Plastic DIP, $12.80 (100). Delivery, six to eight weeks ARO.

Standard Microsystems Corp, 35 Marcus Blvd, Hauppauge, NY 11788. Phone (516) 273-3100. TWX 510-227-8898.

Circle No 373



1M-BIT ROM

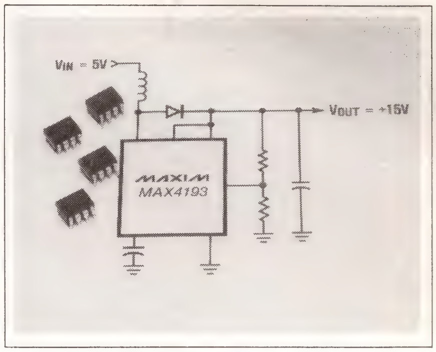
The M5M231000P, a mask-programmable ROM configured as 131,072 words×8 bits, is available with access times of 250 or 300 nsec. Developed with n-channel silicon-gate MOS technology, the chip's access times and power consumption are comparable to the company's 256k-bit ROM. It's housed in a 28-pin plastic DIP. $25 (OEM qty); a mask charge of $2500 is required. Delivery, 10 to 12 weeks ARO.

Mitsubishi Electronics America Inc, 1050 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 730-5900. TWX 910-339-9549.

Circle No 374

REGULATOR IC

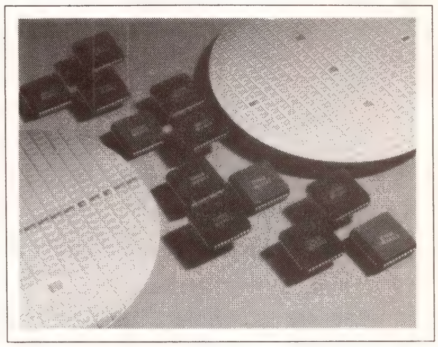
The MAX4193 monolithic CMOS dc/dc converter increases the efficiency of discrete dc/dc-converter circuits in the 5 mW to 5W range, according to the company. An on-board power MOSFET has an on-resistance of 4Ω and a maximum current rating of 375 mA (no base drive current is required). The IC's standby current is 5 μA; operating current at 40 kHz is 200 μA max



(80 μA typ), independent of the MOSFET's output duty cycle. The manufacturer claims that the product can achieve 80% efficiency in most applications. It operates over an input voltage range of 2.4 to 16.5V. You can choose from three temperature ranges: 0 to 70°C, −40 to +85°C, and −55 to +125°C. $1.72 to $5.80 (100).

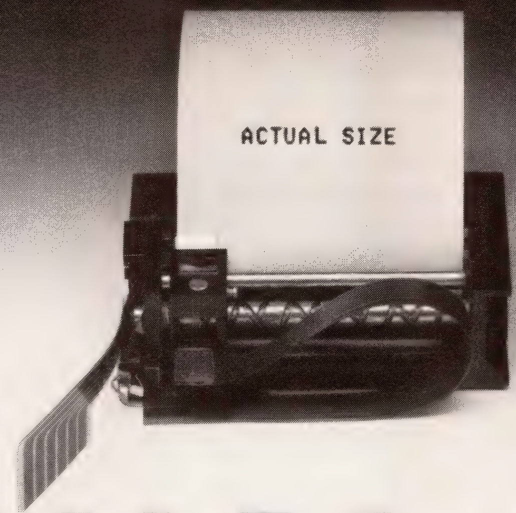
Maxim Integrated Products, 510 N Pastoria Ave, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 375



EL DRIVERS

This second-generation electroluminescent-display-driver chip set replaces many discrete components for driving EL-display panels. Using this chip set, you can reduce the pc-board space required for large, flat-panel displays; achieve brighter displays with sharper resolution; and reduce overall power dissipation. The Si9551 and Si9552 row drivers (rated at 225V and 50 mA) and Si9553 and Si9554 column drivers (with sink and source capability to 15 mA) are pin and function compatible with existing 32-channel driver circuits. The ICs operate over the military temperature range



Add A Lot of Character To Your Lines.

With a character height of 2.4 mm, these 5 x 7 Dot Matrix Printers will produce alphanumerics in any language, with the best looking characters available. And that's just the beginning of Seiko Instruments compact thermal printers.

Quiet performance, low power consumption and an extremely reliable, maintenance-free operational minimum of 500,000 lines MCTF. A lot of characters at prices as impressive as their performance.

Seiko's versatile, high-quality MTP series are perfect for calculators, measuring instruments, small computer terminals, data loggers, telephones, medical instruments... just about every application.

For added flexibility, add the C-MOS MTPI-CC interface board. Or, turn a lot of characters into a lot of graphics with our MTPI-GNP (parallel) or MTPI-GNS (serial) interface boards. Each board is designed to meet a variety of data output sources.

Item \ Model		MTP102		MTP201		MTP401	
		13	16	20	24	32	40
Number of columns		13	16	20	24	32	40
Printing Speeds (CPS)		24		19		24	
Character size (HxW)	mm (in)	2.4x1.4 (.09x.06)	2.4x1.1 (.09x.04)	2.4x1.5 (.09x.06)	2.4x1.3 (.09x.06)	2.4x1.4 (.09x.06)	2.4x1.1 (.09x.06)
Dimensions (WxDxH)	mm (in)	48x31x13.8 (1.89x1.22x0.54)		70x34x14.4 (2.76x1.34x0.57)		91.5x35.5x20 (3.60x1.40x0.79)	
Weight	g (oz)	Approx. 35 (1.25)		Approx. 40 (1.42)		Approx. 50 (1.78)	

So, for your new lines or existing lines, specify Seiko Instruments Thermal Printers... it will add a lot of character and a lot of performance to your designs.

SEIKO INSTRUMENTS U.S.A., INC.
2990 W. Lomita Blvd.
Torrance, CA 90505
Telephone: (213) 530-8777
TWX: 910-347-7307 SEIKO INST. TRNC.
FAX: (213) 539-8621

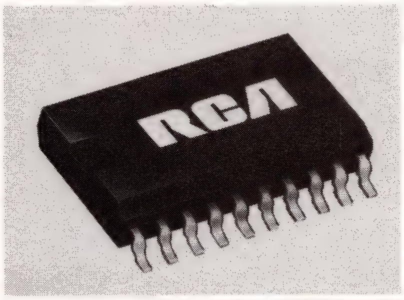
SEIKO INSTRUMENTS

CIRCLE NO 125

and are available in a ceramic quad 44-pin J-lead package (AM suffix), a plastic quad 44-pin LCC (CN suffix), or in chip form. $5.40 to $29.02 (1000).

Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000.

Circle No 376



OCTAL BUFFERS

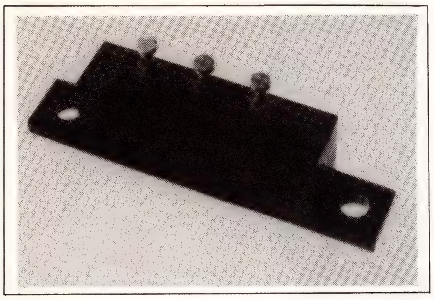
The 54/74HC and 54/74HCT families of high-speed CMOS octal buffer/line driver ICs offer buffered inputs and 3-state outputs that can drive 15 LS TTL loads. The 54/74HC versions, for systems using all-CMOS ICs, operate between 2 to 6V dc; the 54/74HCT versions are compatible with LS TTL bipolar-logic devices and operate over 4.5 to 5.5V dc. The CD54/74HC/HCT540 and 541 ICs feature inverting and noninverting outputs, respectively. Typical propagation delay is 9 nsec at 5V, with a 15-pF load on the output. The CD54/74HC/HCT240 (inverting) and CD54/74HC/HCT241 and 244 (noninverting) ICs use the same pinouts. The chips have typical propagation delay times of 8 nsec (240) and 9 nsec (241 and 244). $0.99 to $1.06 (100).

RCA Solid State Div, Rte 202, Somerville, NJ 08876. Phone (201) 685-7460.

INQUIRE DIRECT

RECTIFIERS

The SHCDA05HE Series of center-tap doubler assemblies can operate as full-wave output rectifiers for high-current and very fast switch-



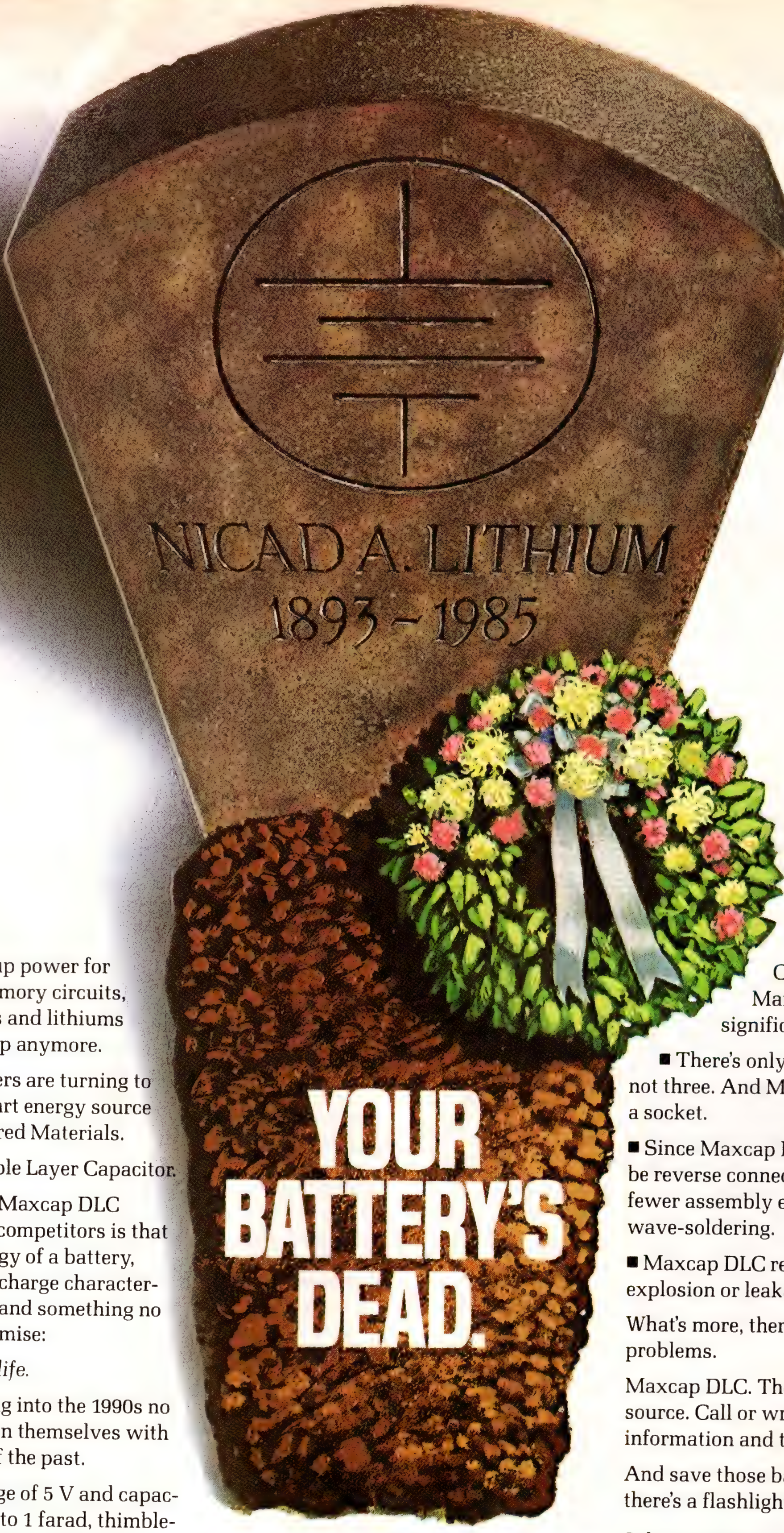
ing power supplies. Positive or negative outputs are available. The devices supply 44A of output current, which, according to the manufacturer, is more than twice the output of industry-standard units. Moreover, virtually no increase in mounting space is necessary. Turn-off time is 30 nsec. The series comes in 50, 100, and 150V versions. 50V version, $57 (100). Delivery, 10 to 12 weeks ARO.

RSM Electron Power Inc, Sensitron Semiconductor Div, 221 W Industry Ct, Deer Park, NY 11729. Phone (516) 586-7600.

Circle No 378

STANDARD CELLS

This family of 2- and 3-μm standard cells (the MSM90000 and MSM91000, respectively) uses the manufacturer's concept of conversion transparency. The silicon-gate, dual-layer-metal design process and databases are compatible with the manufacturer's line of gate-array products. The cells offer more than 84 functional logic cells and 38 macro blocks, which include several μPs and microcontrollers, a bus con-



As backup power for CMOS memory circuits, the ni-cads and lithiums just don't measure up anymore.

Now, circuit designers are turning to a new, state-of-the-art energy source from Sohio Engineered Materials.

The Maxcap™ Double Layer Capacitor.

What distinguishes Maxcap DLC from its antiquated competitors is that it gives you the energy of a battery, the rapid charge-discharge characteristics of a capacitor, and something no battery can ever promise:

Virtually unlimited life.

So designers working into the 1990s no longer have to burden themselves with power sources out of the past.

At its nominal voltage of 5 V and capacitance values of 0.01 to 1 farad, thimble-size Maxcap DLC can be charged and discharged indefinitely without maintenance or replacement. Since there's no need for access, equipment can be made smaller and simplified. You can also reduce backup circuit and assembly costs.

Compared to batteries, Maxcap DLC delivers these significant cost savings:

- There's only one extra component, not three. And Maxcap DLC doesn't need a socket.
- Since Maxcap DLC is nonpolar, it can't be reverse connected, so you'll have fewer assembly errors. And you can use wave-soldering.
- Maxcap DLC requires no toxicity, explosion or leakage safeguards.

What's more, there are no disposal problems.

Maxcap DLC. The timeless energy source. Call or write for complete information and technical details.

And save those batteries. Somewhere, there's a flashlight that can use them.

Sohio Engineered Materials Company
Semiconductor Products Division
P.O. Box 664
Niagara Falls, NY 14302
716/278-3954

SOHIO

Sohio Engineered Materials Company

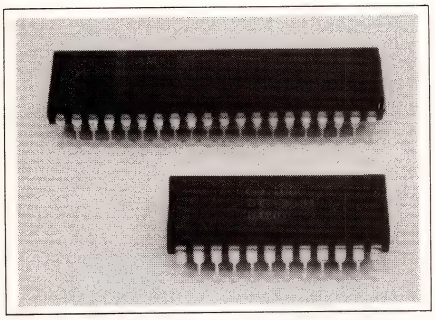
Maxcap DLC shown actual size above.

CIRCLE NO 127

troller, a digital signal processor, a high-speed A/D converter, a DTMF, an LCD controller, and several RAMs and ROMs. The MSM91000 uses a single-well CMOS process and has a 2.7-nsec typ gate delay; the MSM90000 uses a double-well process and features a 2.2-nsec gate delay. Operating temperature spans −40 to +85°C. In a conventional plastic package, cost is $0.15 to $0.25 per gate (100,000).

Oki Semiconductor, 650 N Mary Ave, Sunnyvale, CA 94086. Phone (800) 336-3555; in CA, (408) 720-1900. TWX 910-338-0508.

Circle No 379

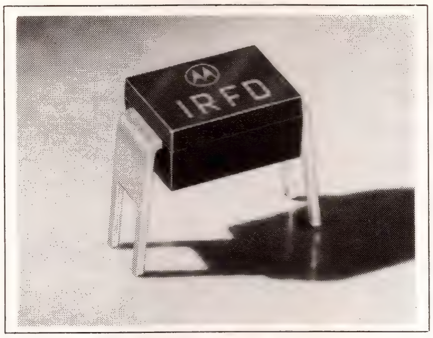


CONTROL IC

A mask-ROM version of the MCC-3000 motion-control chip set consists of a 40- and a 24-pin DIP. The μP-based chip set performs the functions of a dedicated position and velocity controller, freeing the host from the time-intensive task of closed-loop dc-motor control. You can program the chip set via an RS-232C port or an 8-bit μP bus. The IC can perform velocity profiling with programmable acceleration and speed, absolute or relative positioning, and position and status reporting. It can accept commands from a remote computer and inputs from local switches for starting and stopping motion, homing, and error protection. No velocity feedback from a tachometer is necessary. $49 (10,000). Delivery, six weeks ARO.

Galil Motion Control Inc, 1928A Old Middlefield Way, Mountain View, CA 94043. Phone (415) 964-6494. TLX 171409.

Circle No 380

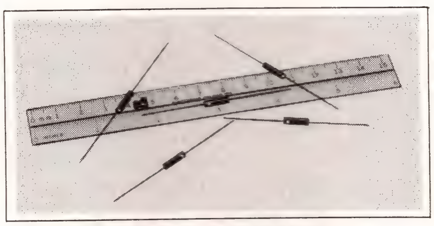


POWER MOSFETs

This line of medium-power TMOS field-effect transistors comprises the single-FET IRFD1Z0/1Z3, IRFD110/113, and IRFD9120/9123 devices and the quad-FET IRFE110/113 and IRFE9120/9123 devices. Single FETs come in 4-pin plastic DIPs, and quad FETs come in 16-pin DIPs. Power dissipation is 1W/device (3W max per package). All devices operate from −55 to +150°C. Single configurations, $0.51 to $2.04; quad configurations, $5.94 to 14.04 (100). Delivery, four to six weeks ARO.

Motorola Semiconductor Products Inc, Box 20912, Phoenix, AZ 85036. Phone (602) 244-4238.

Circle No 381

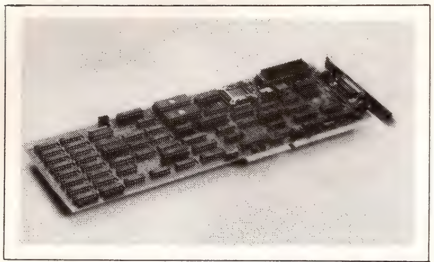


RECTIFIER DIODES

This manufacturer has expanded its Series EF/RF miniature diodes to include units with peak reverse voltages from 1000 to 12,000V and with currents from 80 to 500 mA. You can choose diodes with 150-nsec, 250-nsec, and standard recovery times. Surge ratings spec 8 to 35A. The diodes measure 0.380×0.0160 in. with 1-in. leads. Approximately $6 (1000).

Electronic Devices Inc, 21 Gray Oaks Ave, Yonkers, NY 10710. Phone (914) 965-4400.

Circle No 382

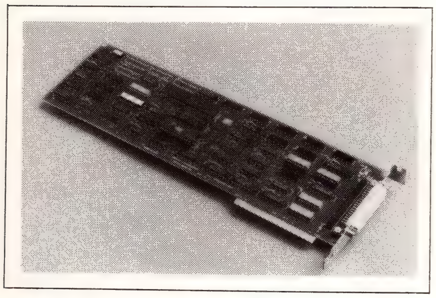


ETHERNET CONTROLLER

You can link the IBM PC/AT to Ethernet using the NP600 Ethernet protocol processor board, a single-board communications processor that plugs into the PC/AT bus. The processor combines an 80186 μP with an 82586 VLSI Ethernet controller chip. The 80186 implements protocol processing for information exchanges between computers on the network; the 82586 handles CSMA/CD link-management procedures and several link-diagnostic functions. It comes with 128k bytes of memory, 16k bytes of EPROM, and diagnostics, including self-testing at power-on. $1150.

Micom Systems Inc, Box 8100, Simi Valley, CA 93062. Phone (805) 583-8600. TWX 910-494-4910.

Circle No 427

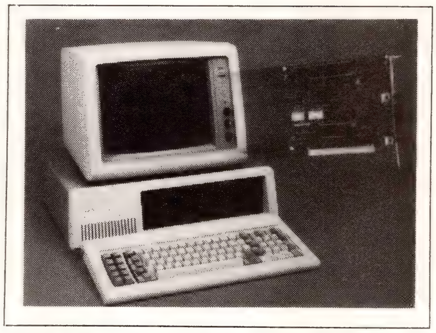


SCSI ADAPTER

The IB02 host adapter connects an IBM PC to SCSI peripherals. Housed on a pc board, the adapter contains a protocol controller and implements full SCSI protocol. The adapter integrates 5¼-in. Winchester disk drives and/or ¼-in. cartridge-tape drives into a SCSI system. Its disconnect/reconnect feature allows devices on the bus to disconnect and then reconnect when they have completed their tasks. The adapter includes onboard memory; 6k bytes of ROM and 2k bytes of RAM map the memory and initialize the SCSI device. You can attach as many as seven controllers, each of which can connect to as many as eight 5¼-in. Winchester disk drives with capacities of >110M bytes. $395.

Emulex Corp, Box 6725, Costa Mesa, CA 92626. Phone (800) 368-5393; in CA, (714) 662-5600.

Circle No 428



INTERFACE BOARD

The MBC-488 is an IEEE-488 interface board for the IBM PC, PC/XT, PC/AT, and compatible computers. The board fits into a PC expansion slot; an IEEE-488 connector extends out the rear of the PC. A software driver/interpreter is included on a floppy disk. It operates as a DOS-resident driver, so you can interface IEEE-488 commands to a variety of high-level languages, including Basic, Fortran, Turbo-Pascal, and C. The GPIB can handle as many as 14 other talker/listener devices. $275, including software.

MetraByte Corp, 254 Tosca Dr, Stoughton, MA 02072. Phone (617) 344-1990. TLX 503989.

Circle No 429

68020 BOARD

The D020 system accelerator turns a 68000-based computer into a 68020/68881 development system. This plug-in replacement for the 68000/68010 μP contains a 68020 and a socket for a 68881 floating-point coprocessor. It runs Unix System 5.2. Because the board is compatible with object code that the 68000 family runs, you can improve system performance while optimizing program code for future 68020 processor boards, according to the manufacturer. $995.

Synergy Microsystems, 1820 Cambridge Ave, Cardiff, CA 92007. Phone (619) 753-2191.

Circle No 430

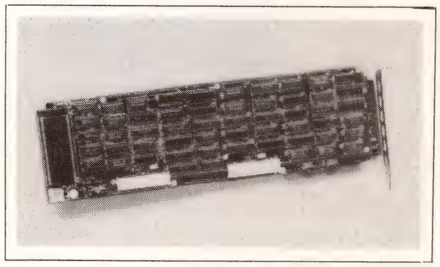


IMAGE COMPRESSOR

The Compressit PC add-on board reduces the space needed to store bit-mapped images. The compressor removes redundant information and encodes the data. A continuous-tone gray-scale or color image will compress between 4:1 and 8:1, and B&W text or line drawings from a scanner compress between 25:1 and 50:1 typ. The compressor requires one slot in the IBM PC expansion bus. According to the manufacturer, it will execute compression algorithms approximately 10 times faster than an assembly-language program on the IBM PC/XT and about four times faster than such a program on the PC/AT. $995.

Chorus Data Systems, Box 370, Merrimack, NH 03054. Phone (800) 624-6787; in NH, (603) 424-2900.

Circle No 431

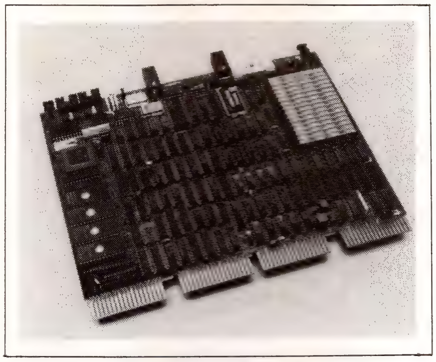
TAPE CONTROLLER

This VME Bus-compatible tape controller, the VME-TC50, works with two ½-in., 9-track tape drives. In addition to 48k bytes of onboard data cache for sustained high data-transfer rates, the controller provides a burst-transfer rate higher than 500k bytes/sec, onboard diagnostics with LED indicator, a real-time calendar/clock, and programming-packet processing. It controls streaming and start/stop tape drives that operate at 800, 1600, 3200, and 6250 bpi. $2000.

Integrated Solutions, 1140 Ringwood Ct, San Jose, CA 95131. Phone (408) 943-1902. TLX 4996929.

Circle No 432

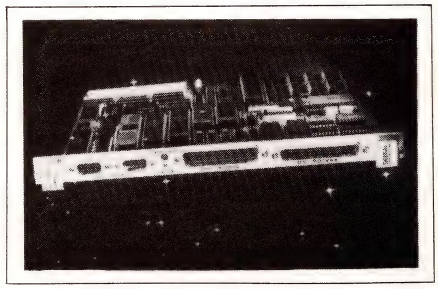
GRAPHICS PROCESSOR



The HSRGB, a graphics front-end processor with RGB output for use with a medium-resolution color CRT, is available for Unibus or Q Bus applications. The processor provides 512k bytes of onboard graphics memory for dual-ported display storage. In VT100 emulation mode, the board allows you to scroll VT100 text independently on the color screen in a split-screen format; you don't need a separate control terminal to operate the color console. The board performs over 50 standard graphics commands, including system control and such graphics functions as draw circle, ellipse, square, area fills, and pixel, as well as archiving. With DMA-device drivers, the processor operates under DEC's RSX11-M+, RT-11, and VMS operating systems. $4350.

MDB Systems Inc, 1995 N Batavia St, Orange, CA 92665. Phone (714) 998-6900. TWX 910-593-1339.

Circle No 433



VME BUS BOARD

The SL-1000 dual-height VME Bus board specs data-acquisition rates as high as 20 kHz. The board provides 16 single-ended or eight differential 12-bit analog inputs with autozero, autorange, and multiple-

input ranges; 32 parallel, programmable I/O lines; a counter/timer; two RS-232C ports; a watchdog timer; and a run/halt/diagnostic indicator. Options include 64k or 128k bytes of local data storage and two 12-bit-resolution analog outputs. $2195.

Serial Lab Products Inc, Box 766, Marlboro, MA 01752. Phone (617) 481-1684.

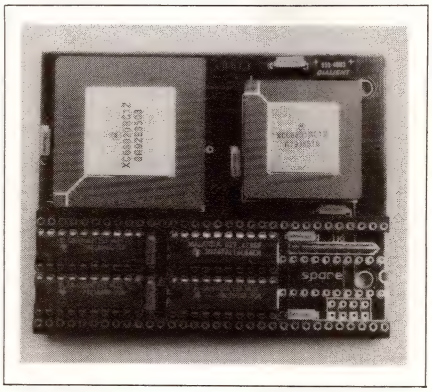
Circle No 434

SCSI CONVERTER

Using the RT-SDA adapter, you can convert either initiator or target single-ended SCSI devices to differential-ended SCSI devices. The converter meets ANSI spec X3T9, and it allows you to increase the SCSI cable length from 20 to 82 ft. You can power the converter from the initiator or target device's terminator or via an onboard power connector; target and initiator sensing is automatic. The unit measures 3½×6 in. $150.

Rancho Technology, 10238 Monte Vista, Rancho Cucamonga, CA 91701. Phone (714) 987-3966.

Circle No 435



PROCESSOR BOARD

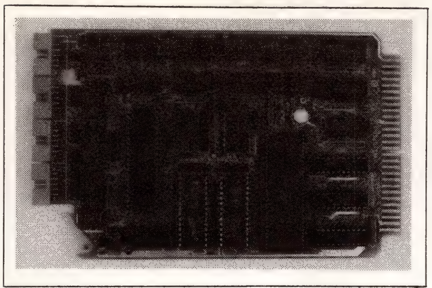
The D020 daughter board provides a 68020 CPU and a 68881 floating-point processor on a pc board that plugs directly into existing 68000/68010 sockets; for most applications, no software changes are required. According to the manufacturer, this combination of components can increase the speed of logical processing throughput by 300% and floating-point processing throughput by several orders of magnitude in arithmetic-intensive applications. The daughter board is available in two versions: D020-0 comes with the 68020; the D020-1 includes the 68020 and the 68881. For both versions, you can choose connector heights of 0.335 or 0.585 in. D020-0, $995; D020-1, $1275.

Io Inc, 2430 N Huachuca Dr, Tucson, AZ 85745. Phone (602) 792-0969.

Circle No 436

STD BUS BOARD

The LPM-SBC5 single-board computer uses the HD64180 Z80-compatible processor, which includes 512k bytes of direct memory ad-



dressing, hardware multiply, two DMA channels, two 28-pin JEDEC memory sockets, two 16-bit timers, and four RS-232C or RS-422 channels. It also features automatic dynamic-refresh generation, a wait-state generator, a watchdog timer, and three sleep modes. The board is available with NMOS/TTL I/O capability for the STD Bus (Model MCM-SBC5) and all-CMOS capability for the CMOS STD Bus (Model LPM-SBC5). Two DMA controllers are included. The board generates a refresh signal to support dynamic RAMs. The programmable wait-state generator is available for slow memory and I/O devices. The LPM-SBC5 version operates over −40 to +85°C; the MCM-SBC5 model operates over 0 to 60°C. LPM-SBC5, $450; MCM-SBC5, $395 (4-MHz versions).

Winsystems Inc, Box 121361, Arlington, TX 76012. Phone (817) 274-7553.

Circle No 437

MOTION CONTROLLER

The μP-based DMC-430, a 3-axis programmable motion controller on an IBM PC-compatible card, handles such motor-control functions as precision positioning, velocity profiling, and status reporting. The controller accepts position feedback from an incremental encoder; no tachometer feedback is required. Speed ranges as high as 30,000:1, and position resolutions of <1 μm are possible. $1645.

Galil Motion Control, 1928-A Old Middlefield Way, Mountain View, CA 94043. Phone (415) 964-6494. TLX 171409.

Circle No 438

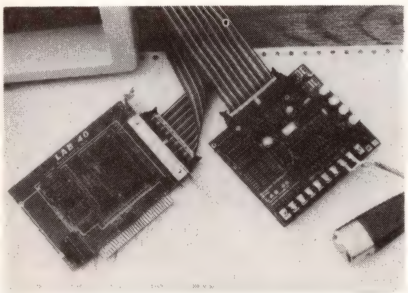
1-BOARD COMPUTERS

The iSBC 386/20 CPU board is based on the Multibus I architecture; the iSBX 386/100 CPU board uses Multibus II architecture. Each board provides onboard cache memory, an 80287 or 80387 (when available) numeric coprocessor, high-speed memory interface to accommodate as much as 16M bytes of system memory, an interface to the iSBX bus for I/O, and two sock-

ets for EPROM. The 386/20 board uses a 32-bit-wide bus for data transfers between the CPU and the dual-port memory and a 16-bit bus for transfers over the Multibus I or iSBX Bus. Both boards run iRMX 286/386, Xenix, and Unix System V operating systems as well as proprietary operating systems written for the 8086 or 80286 CPU. $3860 (100).

Intel Corp, Literature Dept W253, 3065 Bowers Ave, Santa Clara, CA 95051. Phone (408) 987-8080.

Circle No 439



µC INTERFACE

The Lab 40 system is a circuit board, or bus generator, which connects to the host computer and drives a 40-connector ribbon-cable bus. The bus generator interacts with function modules, which can be circuits from this company, user-built circuits, or compatible circuits from other manufacturers. You can place as many as eight function modules on a 100-ft-long ribbon cable. The bus-generator cards are available for the IBM PC and Apple II; development software is included. $175.

Computer Continuum, 75 Southgate Ave, Suite 6, Daly City, CA 94015. Phone (415) 755-1978.

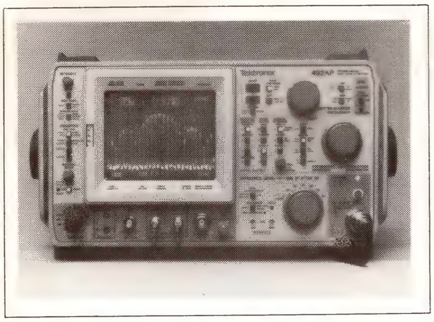
Circle No 440

SINGLE-BOARD µC

The 80186 µP-based VS-186 is a PC-DOS-compatible, single-board computer that allows you to install as much as 512k bytes of ROM in eight JEDEC 28-pin EPROM sites. The board can accommodate as much as 1M byte of parity-checked RAM. In addition to a socket for the 8087 math coprocessor, the board provides two serial ports, a programmable parallel port, a Centronics printer port, a SASI/SCSI interface for disk and tape drives, four iSBX expansion connectors, and a processor bus extension that permits communication with other bus structures. The board measures 8½×11 in. $950.

Virtual Systems Inc, 1500 Newell Ave, Suite 406, Walnut Creek, CA 94596. Phone (415) 935-4944.

Circle No 441

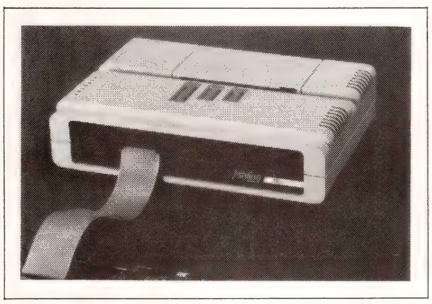


325-GHz ANALYZERS

The Models 492A and 492AP 325-GHz spectrum analyzers have a signal-processing ability that allows them to sort continuous-wave, pulse, and other signals. The instruments' dot markers are accurate to 0.01%. The units provide selectable reference units of dBm, dBV, and dBmV. Moreover, you can store nine front-panel setups in nonvolatile memory. A MATE/CIIL interface for military applications is optional. From $27,290. Delivery, 12 weeks ARO.

Tektronix Inc, Box 1700, Beaverton, OR 97005. Phone (800) 547-1512; in OR, (800) 452-1877.

Circle No 383

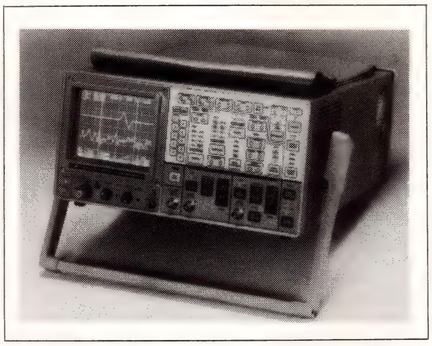


8051 EMULATOR

The A51 emulator for the 8051 single-chip µP family incorporates a PROM programmer that handles 2716 through 2764 devices as well as the 8751. You control the emulator with an IBM PC. The PC-compatible assembler handles 2000 lpm. A windowing screen editor allows you to compare files of captured data with your source code. The emulator's software includes a macro, or command-file, capability. The emulator operates as fast as 12 MHz in real time and comes with 8k bytes of emulation memory. You can set hardware breakpoints on as many as 48,000 memory locations. From $5750.

Ashling Microsystems Inc, 542 Lakeside Dr, Suite 2, Sunnyvale, CA 94086. Phone (408) 720-9131.

Circle No 384



DIGTIZING SCOPE

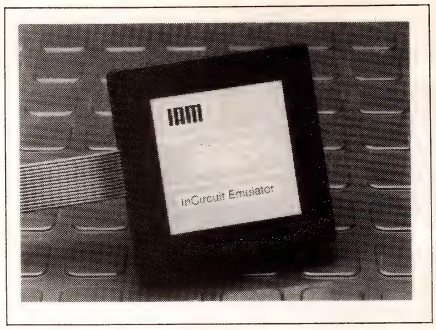
The dual-channel Model DS-6121 is a 100-MHz analog scope that digitizes incoming signals at 40M samples/sec. The unit has four waveform memories. After capturing a signal, the instrument can add, subtract, multiply, and average stored waveforms; it also compares a captured waveform with a stored waveform. You can control all the instrument's functions via the IEEE-488 bus. Cursors provide direct readouts of voltage, voltage ratio, time, and phase. $5550. Delivery, eight weeks ARO.

Iwatsu Instruments, 430 Commerce Rd, Carlstadt, NJ 07072. Phone (201) 935-5220.

Circle No 385

MINIATURE EMULATORS

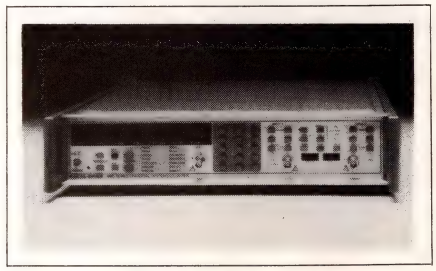
Measuring 3×3×½ in., in-circuit emulators in this series require only a nonintelligent terminal for operation. The units draw their power from the circuit under test; optional external supplies are available for some models. The emulators provide such standard features as the ability to examine and change memory locations, breakpoints, and hex and ASCII displays. Emulators in the series can assemble and disas-



semble µP instructions; models are available for the 8085, 8088, Z80, and NSC800 µPs. From $500.

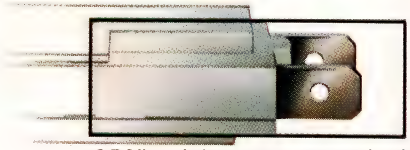
IAM, Box 2545, Fair Oaks, CA 95628. Phone (916) 961-8082.

Circle No 386



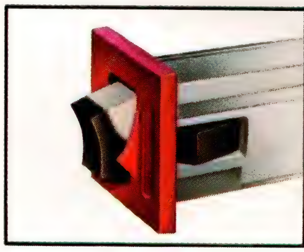
UNIVERSAL COUNTERS

These two universal counter systems, the 1995 and the 1996, suit large ATE applications. The 1995 features two 200-MHz input channels with independent start/stop control on each channel. You can select an input impedance of either 50Ω or 1 MΩ. The 1996 adds a fuse-protected third input for measurement to 1.3 GHz. In both models, you can reverse the internal assembly and consequently make connections to the rear or front panel. Data-output rate is 150 readings/second. Positive- and negative-peak detectors provide separate readouts of peak and peak-to-peak signal characteristics. These detectors also determine the signal amplitude for autotrigger, slew-rate, and rise/fall-time calculations. The 10-digit display presents frequency and period resolution to nine digits in 1 sec over the entire frequency range. A single-shot time-interval resolution of 1 nsec permits examination of rise/fall and propagation times. You can use averaging to

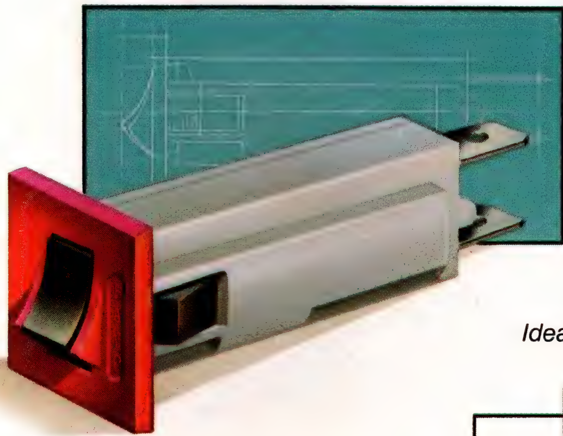


• .250" quick-connect terminals make wiring easy.

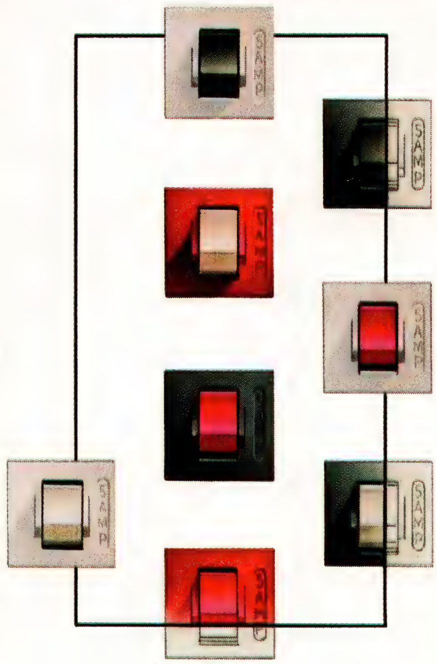
• Trip indicator warns of a possible circuit problem. Choice of red or white.



• Special molded clips snap securely into standard ⅝" panel cutouts. No redesign or repunching.



• Variety of bezel and button colors permit color coding of circuits. Ideal for convenient up front control panel location.



P&B's new snap-in circuit breakers end fuse replacement worries.

Our W28 series thermal circuit breakers fit the same cutout as many ⅝" fuseholders. And from 0.25 through 15 amps these UL recognized and CSA certified breakers do the same job as fuses. Only better. When the W28 trips, an indicator pops out to warn of a possible circuit problem. After the trouble is located and corrected, the W28 can be reset by simply pushing a button. But it can't be pulled out to disconnect the circuit.

Easy To Install. Wherever you presently use glass cartridge fuseholders, W28s can replace them without panel redesign or repunching. Think about putting them out front. That way they're easily accessible and their attractive appearance will add to your product's appeal. W28 breakers can be prewired and then snapped securely into the panel from the front.

Helps Sell Your Product. For everything from home entertainment equipment to medical instruments to industrial test gear, W28 breakers add selling points to your product. Good looks. The convenience of not searching for fuses. Protection against improper fuse rating substitutions. And they save the cost and trouble of maintaining a fuse inventory.

Write For Our Catalog. Find out about the economical W28 and our full line of magnetic and thermal circuit breakers. They're available off-the-shelf from authorized P&B distributors backed by our sizable factory inventory. Or contact your local P&B sales representative. Potter & Brumfield Division AMF Incorporated, 200 Richland Creek Drive, Princeton, Indiana 47671.
Call toll free 800/255-2550.

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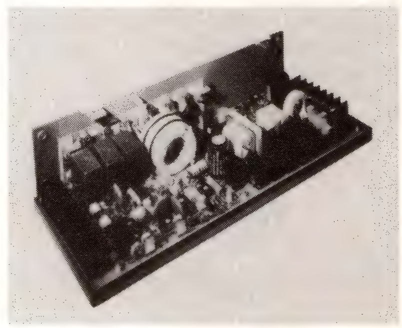
CIRCLE NO 134

increase resolution to 100 psec. IEEE-488 programmability allows remote system control. 1995, $3750; 1996, $4500. Delivery, eight weeks ARO.

Racal-Dana Instruments Inc, Box C-19541, Irvine, CA 92713. Phone (714) 859-8999. TLX 678341.

Circle No 387



BATTERY SUPPLIES

The LPS Series of battery-backed, 400W switching power supplies spec 98% efficiency min for on-line operation and 85% min efficiency when powered by their batteries. Units in the series comprise a dc/dc converter, batteries that supply five minutes of full-load operation, a battery charger, and an isolation bridge. The series permits transfers to and from battery power without the aid of active sensors and produces no glitches on its outputs during a transfer. Both the charger and inverter are protected against overloads, overtemperature, and short circuits. The supplies come in two models: the $435 LPS-40 master and $360 LPS-41 slave, which doesn't include the charger.

Lambda Electronics, 515 Broad Hollow Rd, Melville, NY 11747. Phone (516) 694-4200.

Circle No 388

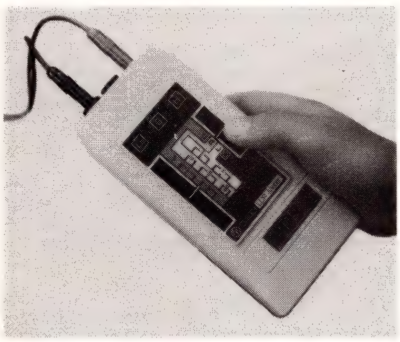
PROGRAMMER MODULE

The M77 adapter module for the company's Prompro-XP and Prompro-8X PROM programmers handles Texas Instruments' TMS-7742 single-chip μP. The unit is suit-

able for both program-development and production applications. Model M77, $150.

Logical Devices Inc, 1321 NW 65th Pl, Fort Lauderdale, FL 33309. Phone (800) 331-7766; in FL, (305) 974-0975. TLX 383142.

Circle No 389



HANDHELD LCR METER

This battery-powered, 20-range LCR meter has a 3½-digit LCD and positive-action slide switches, and it comes in a plastic case. Six inductance ranges span 2 mH to 200H; seven capacitance ranges cover 200 pF to 200 μF; and seven resistance ranges extend from 20Ω to 20 MΩ. Depending on the measurement range you select, the meter operates at a frequency of 1 kHz or 100 Hz. No adjustment or balancing is necessary. A limited output voltage protects electrolytic capacitors and other sensitive devices during measurement; the meter is fuse-protected against accidental application of 250V ac or dc (max), either from charged capacitors or to any terminal. The instrument case has nonslip rubber feet and a fold-out stand for benchtop use. $470.

Biddle Instruments, 510 Township Line Rd, Blue Bell, PA 19422. Phone (215) 646-9200.

Circle No 390

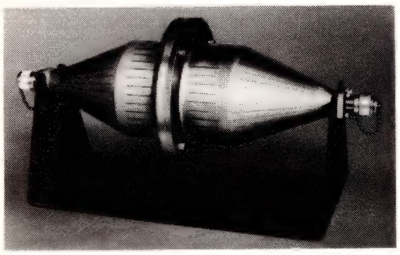
BIT-SLICE DEVELOPER

The DS3700 Emulyzer works with all microprogrammmed processors, including the 29116, 74AS888, and 29300 families and the soon-to-be-introduced AMD 29400 family. The system comprises a 10-nsec memory emulator with a guaranteed access time at the target system of less than 25 nsec, and a 35-MHz logic-state analyzer/performance monitor with triggering and data acquisition. When combined with the company's CS Series workstation, the unit forms a complete stand-alone development system. Alternatively, you can connect the system to a mainframe computer (eg, a VAX) or to an IBM PC. The company provides software, including a relocatable and linkable macro-meta-assembler. Various writable-control-store, memory-emulation modules and logic-analyzer modules provide a choice of emulation-memory

speed and depth. You can configure memory depths from 1k to 64k bits and as wide as 512 bits. From $12,000.

HiLevel Technology Inc, 18902 Bardeen, Irvine, CA 92715. Phone (800) 445-3835; in CA, (800) 752-5215. TLX 655316.

Circle No 391



COAX TEST CELL

Designed to test the effectiveness of RF shielding materials, the SET-19 transmission-line cell simulates the wave-propagation characteristics of a coaxial transmission line. With RF power applied, you can accurately measure levels with a power meter, a spectrum analyzer, or other commonly available equipment. Repeatability is guaranteed. The chamber accommodates sample sizes in accordance with ASTM D09.12.14. Operating bandwidth is dc to 3000 MHz; dynamic range is ±100 dB; and nominal impedance is 50Ω. $6600.

Amplifier Research, 160 School House Rd, Souderton, PA 18964. Phone (215) 723-8181. TWX 510-661-6094.

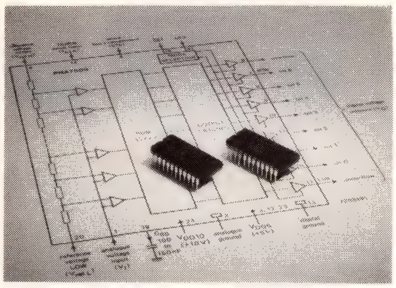
Circle No 392

GANG PROGRAMMER

Series 1000 parallel programmers come with a tool that lets you slide devices in and out of a device manufacturer's tube and directly into the programmers' sockets. This tool cuts the loading time down to 2 sec/device. You can also select programming commands, command options, and device names from scrolling menus. The programmers include other features that minimize down time: socket isolation to identify single-device failures before they affect other sockets; autocalibration of programming and supply voltages; safe power-down in case of power failures; self-diagnostics; and compliance with applicable safety standards. The series works with one-time-programmable MOS and CMOS devices, including PROMs, EPROMs, EEPROMs, and single-chip μPs. Series 1000 adapter modules handle 24-, 28-, 32-, and 40-pin devices. $6500 to $18,000, depending on options.

Data I/O Corp, Box 97046, Redmond, WA 98073. Phone (206) 881-6444. TLX 152167.

Circle No 393



A/D CONVERTER

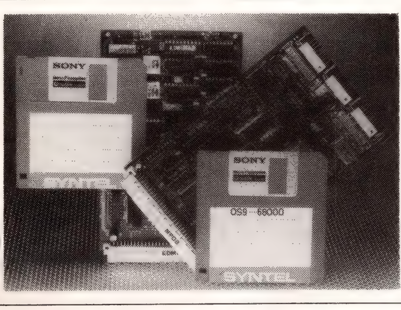
Capable of digitizing an analog signal to 7-bit resolution at a sample rate of 22 MHz, the PNA7509 flash A/D converter features a 10-MHz analog bandwidth. It is fabricated in NMOS technology and dissipates 400 mW typ. The converter has built-in sample/hold circuitry and a 3-state TTL-compatible digital output that you can program for binary code, 2's-complement code, or overflow and underflow conditions. Differential nonlinearity is ± ½ LSB, equivalent to 0.4%. The device requires 5 and 10V supplies and is available in either a 24-pin DIP or a surface-mount version. Approximately $12 (1000) for the plastic-DIP version.

Philips, Elcoma Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 394

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 739-7700.

Circle No 395

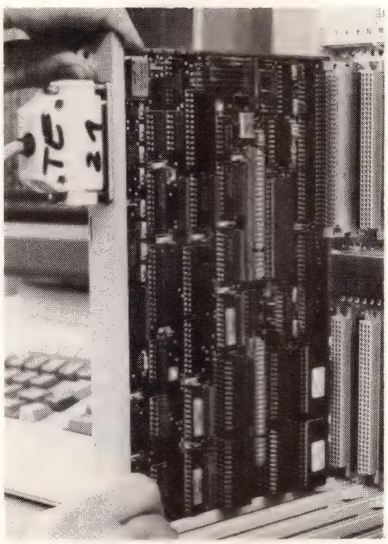


COMPUTER CARDS

These single-Eurocard computer boards suit G64 Bus systems. The SYN-MP08 provides a 68008-based CPU, and the SYN-EDM256 provides 256k bytes of dynamic RAM. The 10-MHz CPU card includes sockets for as much as 128k bytes of EPROM or a mix of EPROM and RAM devices. It also has two RS-232C/RS-422-compatible serial ports and a parallel I/O port. The memory board includes sockets for as much as 128k bytes of EPROM. The OS9/68000 operating system is available for use on a target system or as part of the SMDS-680 development system, which is based on the two computer boards. SYN-MP08, £467; SYN-EDM256, £498.

Syntel Microsytems, Queens Mill Rd, Huddersfield HD1 3PG, UK. Phone (0484) 535101. TLX 51194.

Circle No 396



CPU CARD

The AMS-M7 CPU card for AMS Bus systems runs an 8-MHz 8086 μP and provides sockets for as much as 128k bytes of EPROM and 32k bytes of static RAM. A programmable interrupt controller is provided to enhance the interrupt structure of the 8086. Also included are a V.24/V.28 serial I/O port, a 16-bit timer/counter, and a watchdog timer. You can operate the serial I/O port in a polled or interrupt mode, using synchronous or asynchronous communications protocols at rates between 50 and 19.2k bps. In addition to the AMS Bus interface, the

8.
Meets high technical requirements made nowadays on dual-in-line relays

7.
Low power consumption
Extremely low power consumption of only 75 mW without fixed polarity of current means a lower circuit power demand and less heat dissipation.

6.
Broad switching range
Reliable switching from low-level signals to 150 V/1.25 A at 30 W/50 VA, also withstanding cable discharge.

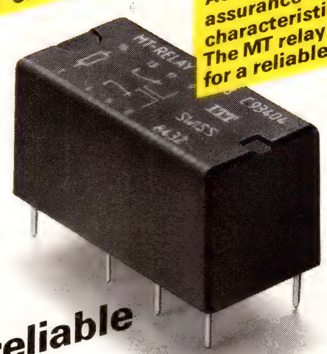
5.
Dielectric strength
Increased protection of circuitry and systems by resistance against surge voltage of 1500 V (10/700 μsec) or 1000 V (1.2/50 μsec).

4.
Broad ambient temperature range
Wide application range at ambient temperatures from −55 °C to 70 °C.

3.
Modular design
Increased reliability by effective intermediate operational checks during production process.

2.
Easy workability
Meets broad range of soldering equipments and automatic washing process thanks to solderability of 10 sec/260 °C or 3.5 sec/350 °C and seal integrity for 10 min/75 °C or 20 sec/125 °C.

1.
High reliability
Achieved by an optimum quality assurance system to maintain the characteristics over the lifetime. The MT relay is therefore made for a reliable future.



MT Relay
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ITT's new dual-in-line relay. Manufactured by Standard Telephone and Radio AG Components Division, 8027 Zurich/Switzerland
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For more information and address of your local sales representative contact reader service.

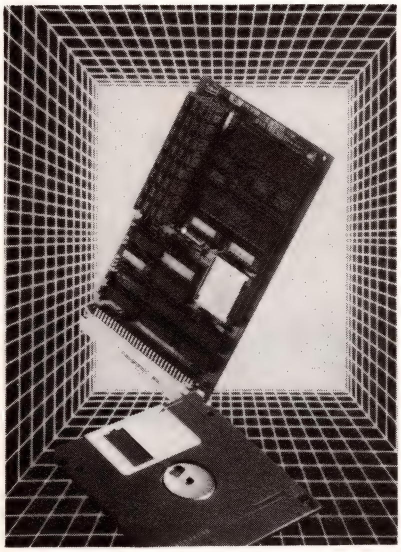
ITT

CIRCLE NO 140

board has two SBX interfaces for expansion boards. A plug-in module, which you insert into the 8086 socket, allows you to add an 8087 math coprocessor. The AMS-M7 board typically draws 2.8A from the 5V supply and operates over 0 to 55°C. DM 2500.

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 397



RUN-TIME SOFTWARE

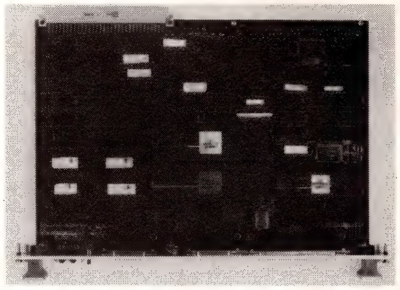
Using the Runtime Library disk pack, you can couple application programs written in C to I/O operations on the STE Bus. Versions of the library routines are available for the company's 80188-based SC88 and Z80-based SCPUB STE Bus CPU cards; these versions run under CP/M-86 and CP/M+, respectively. After program development, the required run-time routines are programmed into EPROM along with the C application program to provide control of the I/O processes. The disk-based software costs £80 and is free from licensing restrictions.

Arcom Control Systems Ltd, Unit 8, Clifton Rd, Cambridge CB1 4WH, UK. Phone (0223) 242224. TLX 817114.

Circle No 398

BOARD COMPUTERS

Series PG-2004 through -2009 VME Bus-compatible single-board computers provide you with either a 68000 or 68010 µP running at 8 or 10 MHz and an optional onboard 68451 memory-management unit. All the computers have space for as much as 128k bytes of onboard ROM, configured as a local memory resource.



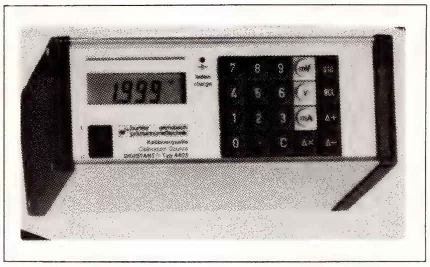
The boards handle seven interrupt levels and have two independent serial I/O ports with RS-232C driver/receiver circuitry. You can program the ports' operating mode, data format, and data rate (data rate spans 50 to 38.4k baud). A programmable parallel port is also provided. $1145 to $1595.

Philips, Industrial & Electroacoustic Systems Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 399

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 739-7700.

Circle No 400



DC CALIBRATOR

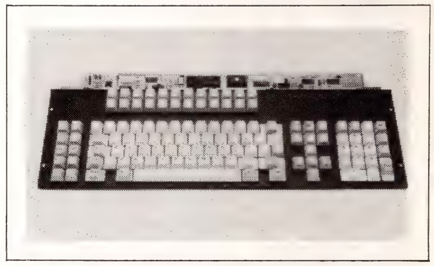
The Digistant 4405A portable calibrator provides dc-voltage and -current calibration sources. The unit has three dc-voltage ranges from 0 to 99.99 mV, 100 to 999.9 mV, and 1 to 11V, with resolutions of 10 μV, 100 μV, and 1 mV, respectively. The output impedance on all voltage ranges is <10 mΩ, and the calibrator is capable of delivering a current of 20 mA maximum at 10V. A single current range spans 0 to 22 mA with a resolution of 2 μA below 20 mA and 10 μA above 20 mA. The current output's voltage compliance is >10V at 20 mA. Output accuracy on all ranges is 0.02% of range, and zero-offset errors are <50 μV or <5 μA. Temperature coefficient on the 11V range is 50 ppm/°C; on all other ranges, it's 75 ppm/°C. The calibrator operates over a temperature range of 0 to 50°C. A numeric keyboard and a 4½-digit LCD display allow you to type the required output value. In addition, 11 internal memory locations, each programmed with a base value and a step value, allow you to generate output staircases using step-increment and -decrement keys. Alternatively, you can set up the base values and step values using the front-panel keyboard. The calibrator is powered by a built-in rechargeable battery or a 115V, 50/60-Hz line supply. The unit measures 9×4×3.5 in. and weighs approximately 3.7 lbs. $698.

Burster Prazisionsmesstechnik, Talstrasse 1-7, 7562 Gernsbach, West Germany. Phone (07224) 6450. TLX 78913.

Circle No 401

Burster Precision Instruments Inc, 125 Wolf Rd, Albany, NY 12205. Phone (518) 458-2640.

Circle No 402



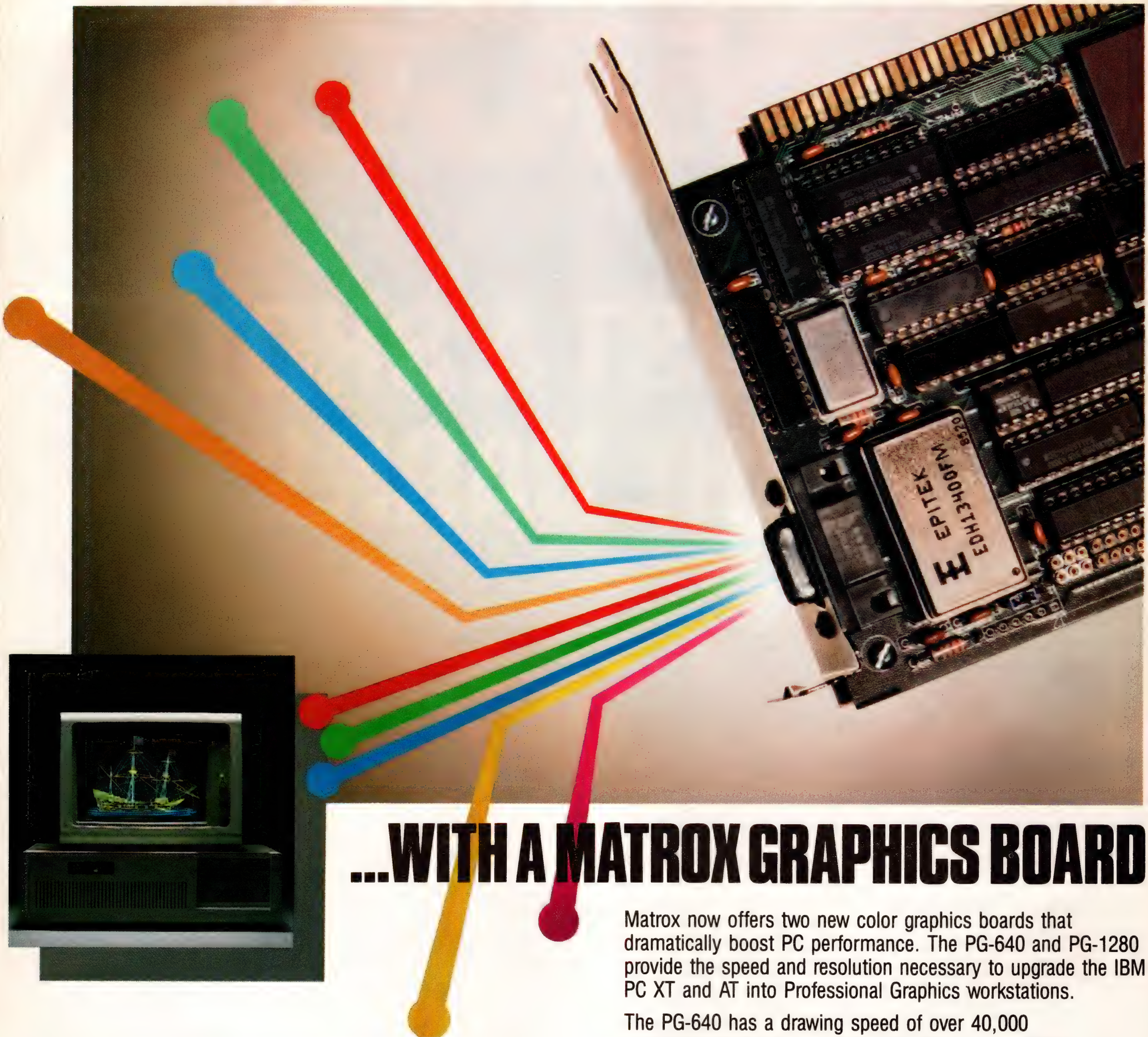
KEYBOARD

This low-profile IBM PC-compatible keyboard assembly suits applications requiring IBM 3179 or 3270 compatibility. The keyboard features 122 capacitively coupled keyswitches, including 24 user-programmable function keys. An onboard μP and EPROM-based firmware let you select output code, autorepeat, and serial-output characteristics. The keyboard is available as a sculptured or stepped array with a choice of more than 30 keycap colors; the keycaps can be color matched to your requirements. The keyboard is manufactured to DIN 66234 standards. The fully encased standard version costs £260.

Alphameric Keyboards Ltd, 6 Manor Way, Old Woking, Surrey GU22 9JX, UK. Phone (04862) 71555. TLX 859131.

Circle No 403

TURBOCHARGE YOUR PC's GRAPHICS



...WITH A MATROX GRAPHICS BOARD

Matrox now offers two new color graphics boards that dramatically boost PC performance. The PG-640 and PG-1280 provide the speed and resolution necessary to upgrade the IBM PC XT and AT into Professional Graphics workstations.

The PG-640 has a drawing speed of over 40,000 vectors/second and an image load speed of 1 million pixels/second. This means complex 640 x 480 pictures are drawn in under a second. The PG-1280 provides even faster picture updates, and displays four times the detail, 1280 x 1024 pixels.

Both the PG-640 and PG-1280 are 100% compatible with IBM's Professional Graphics card, and offer full Color Graphics Adapter emulation. All existing software runs without change.

If you are interested in a 10 times performance boost:

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- **640 x 480 x 8 display (PG-640)**
- **1280 x 1024 x 8 display (PG-1280)**
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H9P 2T4
Tel: (514) 685-2630
Tlx: 05-822798

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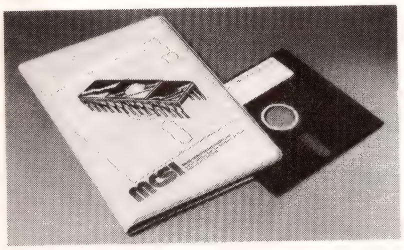
REFERENCE SOFTWARE

The RAM-resident Turbo Lightning and the Turbo Lightning Library can access reference information in a form manageable on a personal computer. Lists of key words are stored in thumbing indexes in RAM; the package accesses information by thumbing through the index files either in RAM or on disk. Pull-down menus provide proofreading and synonym-finding functions; you can check individual words, full screens, or proofread as you type. Words in the thesaurus are organized as nouns, verbs, and adjectives. Using the environment window, you can select WordStar, PFS Write, DOS, Lotus 1-2-3, or other programs; Lightning then pipes in replacement words through the keyboard input buffer. $99.95.

Borland International, 4585 Scotts Valley Dr, Scotts Valley, CA 95066. Phone (408) 438-8400.

Circle No 442



PC BUS UTILITY

PROMdisk allows you to put code, including PC-DOS, networking software, or custom applications in the EPROM on a single-board computer. You can create an image of any file on a diskette and then load it into EPROM. On boot up, the software is read as it would be from a floppy disk; according to the company, the EPROM-based system is faster than a floppy-disk-based system because the code is copied from EPROM into RAM for execution. The software works with the company's PC-compatible single-board computer. It emulates in EPROM as many as four PC disk drives, each of which can accommodate as much as 256k bytes of memory. You can also load additional RAM disks into memory from the EPROM disk drives. One-time license, $1995.

I-Bus Systems, 9235 Chesapeake Dr, San Diego, CA 92123. Phone (800) 382-4229; in CA, (619) 569-0646.

Circle No 443

IMAGE EDITOR

Halovision is an enhanced version of the company's Dr Halo II. Its image editor contains an additional icon to control input from a video camera; you capture an image and then use Dr Halo II's drawing and painting functions to edit and modify the image. The software also provides virtual page, undo, scaling, curve-fitting, image-rotation, image-overlay, snap-grid, menu-switching, and symbol-creation functions. Two versions are available: Halovision A is a display board that works with AT&T's image-capture board and video-display adapter; Halovision I works with Imaging Technology's PC Vision frame grabber. Halovision A, $195; Halovision I, $395.

Media Cybernetics Inc, 7050 Caroll Ave, Takoma Park, MD 20912. Phone (301) 270-0240.

Circle No 444

COMMUNICATIONS

Ptel, a universal binary-transfer program for the IBM PC, PC/XT, PC/AT, and compatible computers running under MS-DOS 2.0 and higher, provides on-line software updating, a line-oriented script language, and forward and backward scrolling. You can access a database of information about the company's other products as well as files of product updates, which you can download and use to update earlier versions of the product. The script language allows you to write a log-on procedure or command program using a text editor; when a file is read, commands are parsed and

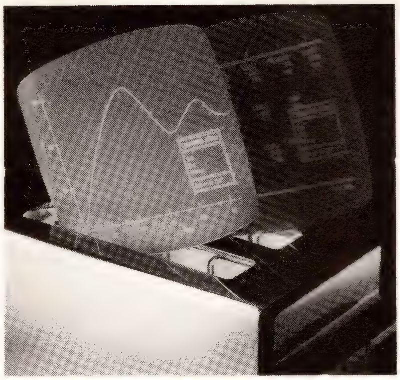
executed as they are encountered. Each script file can call other script files, nested 16 deep, limited only by available memory. You can write intelligent subroutines using an error flag and a general counter. The program works with such protocols as ASCII, XModem, Modem7, Telink, and Kermit. $195.

Phoenix Computer Products Corp, 320 Norwood Park S, Norwood, MA 02062. Phone (617) 762-5030. TWX 710-345-0199.

Circle No 445

SPREADSHEET

The RTSS real-time spreadsheet runs off-screen while you are running other programs on an IBM PC, PC/XT, or PC/AT. With one key sequence, you can call up the program. You can view, scale, or evaluate as many as 1664 sensors. Individual cells can represent raw sensor data, scaled data, or the re-



sults of a formula that uses data from sensors or data contained in other cells. You can scan the digital sensor data in the spreadsheet cells with the cursor keys; when a sensor changes value, its new value is reflected in all cells using that sensor in their formula. Built-in commands are displayed in windows. A graphics window provides a real-time display of any cell. The package works in conjunction with other software, including Labtech Notebook, and it operates with the company's data-acquisition system as well as hardware from Data Translation and Metrabyte. $395; demonstration disk, $25.

Data Motion Corp, 1785 Cortland Ct, Addison, IL 60101. Phone (312) 495-2158.

Circle No 446

DEVELOPMENT SYSTEM

M2SDS, Release 2.0, is a software-development system for the company's Modula-2 language. It includes an incremental compiler, a syntax-directed editor, a linker, 21 library modules, multiple window-editing functions, and 8087 support. The software provides source code for all library modules, the ability to handle long expressions, comment editing facilities, separate color maps, and expanded cut-and-paste functions. You can add new features by downloading from the Modula-2

CIRCLE NO 148

CIRCLE NO 149

PAPST

PAPST — The manufacturer of the PAMOTOR line of fans brings the power of its worldwide expertise to a new nationwide sales network. For more than twenty years, PAMOTOR has been sold under a private label and effective January 1, 1986, will be sold on a national, regional and local level by PAPST MECHATRONIC CORPORATION.

Under the new sales network, PAPST MECHATRONIC CORPORATION will provide the same high quality PAMOTOR products with efficient and expeditious delivery at a lower unit cost.

All ordering information on PAMOTOR will remain the same and additionally, the new low cost DC product line MULTIFAN will become available through the distribution network.

For more information, contact PAPST MECHATRONIC CORPORATION or your local distributor.

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Aquidneck Industrial Park
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(401) 849-8810 Telex: 952092
1-800-242-1520
(Continental USA except MA)
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Ask for operator 31

CIRCLE NO 150

THERE WILL BE A NEW POWER SOURCE DRIVING PAMOTOR.

bulletin board. Release 2.0, $80.88; upgrade for users of M2SDS, $25.

Interface Technologies Corp, 3336 Richmond Ave, Suite 200, Houston, TX 77098. Phone (800) 922-9049; in TX, (713) 523-8422.

Circle No 447

BASIC INTERPRETER

The CB-97 Basic interpreter is an EPROM-resident interpreter that runs on the 8097 16-bit microcontroller on a chip. Reserved words, such as GO SUB and LET, are converted into much shorter tokens, thereby increasing system throughput. It works with integer, floating-point, and string data types. Integer operations ensure utilization of the 8097 hardware. Control constructs in the system allow the software to represent and print constants in hexadecimal; provide logical operators (And, Or, Xor), byte and word peeks, and byte poke; call a user-supplied assembly-language routine; and provide automatic execution upon hardware reset. The software comes on two 2764 EPROMs. $100.

Allen Systems, 2151 Fairfax Rd, Columbus, OH 43221. Phone (614) 488-7122.

Circle No 448

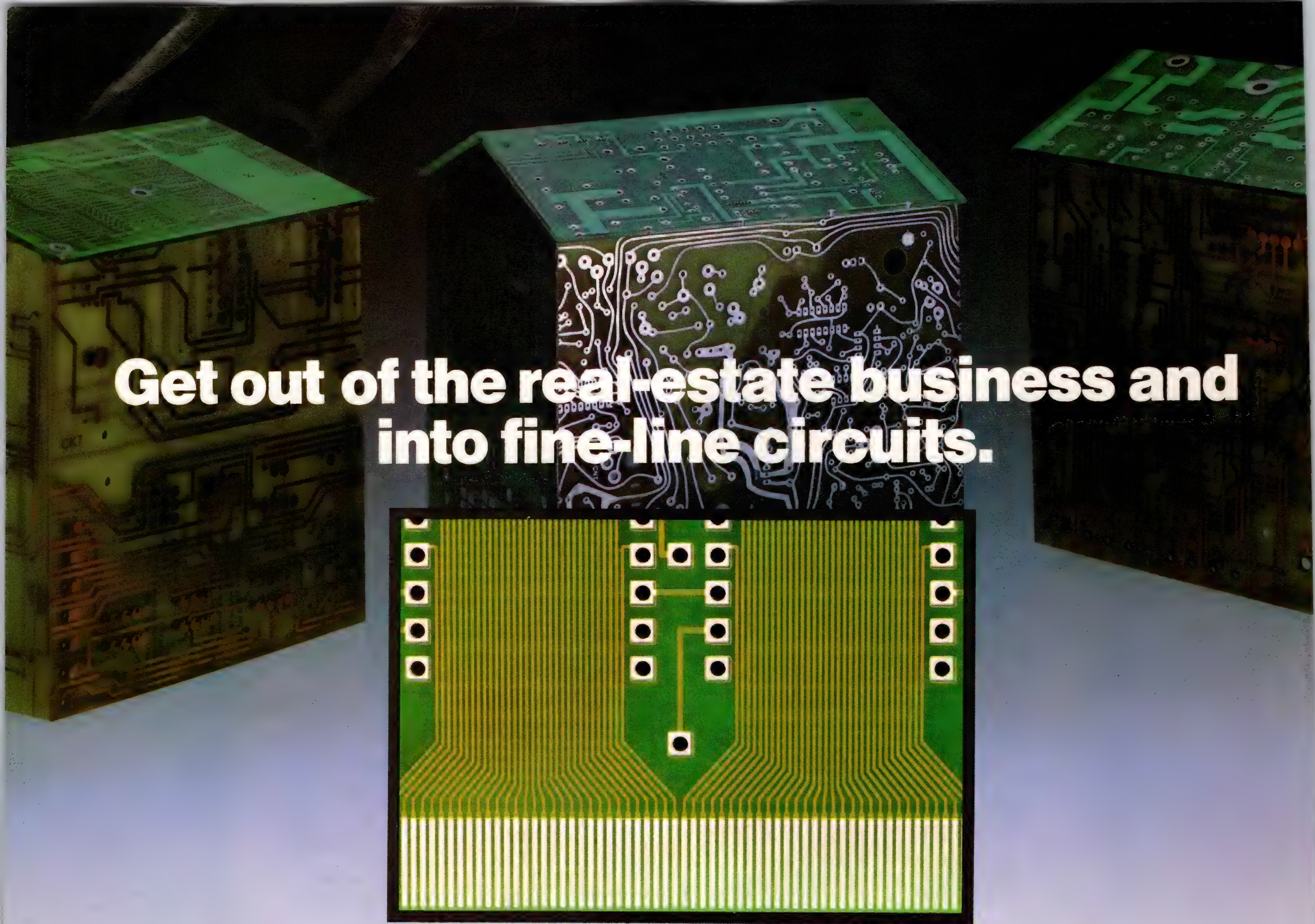
FILTER DESIGN

Dispro, version 1.5, a system for digital-filter design, simulation, and performance analysis, comes in modular form and works with an 8087 coprocessor. You can design IIR and FIR filters and evaluate them for operation in fixed and floating-point arithmetic. The package combines frequency-domain characterization with time-domain simulation functions. Signal generation and spectrum analysis allow you to evaluate digital-filter performance under realistic conditions. Features include representation of coefficients to any word length between two and 24 bits and the ability to screen plots of frequency responses with hard-copy output to the printer. The IIR module designs Butterworth, Chebyshev I and II, and Elliptic function filters; the FIR module designs linear-phase FIR digital filters using the Parks-McClellan-Ramez-exchange and Kaiser-window methods. Two additional modules, Time and Spect, provide time-domain simulation of IIR filters and FFT-based spectral analysis, respectively. Dispro/IIR, $395; /FIR, $295; /Time, $295; /Spect, $295; complete package, $995.

Signix Corp, 19 Pelham Island Rd, Wayland, MA 01778. Phone (617) 358-5955.

Circle No 449

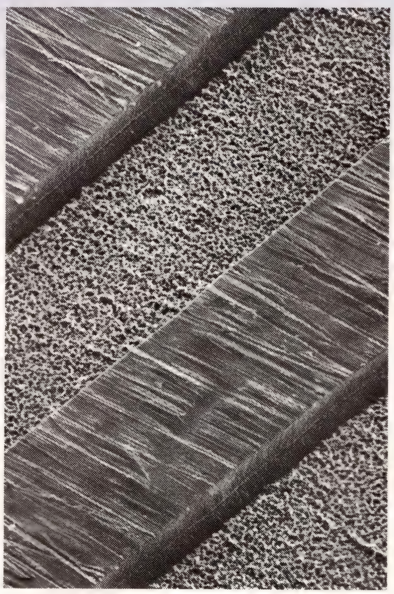
Get out of the real-estate business and into fine-line circuits.



Photocircuits' new Fine-Line Process meets the design engineer's need for high density circuits with increased performance in less real-estate. Circuits with 6-mil lines and spaces and 3 conductors through 100-mil centers are currently being produced. For a major computer company, we're delivering over 2,500 cards per week with 32 traces between 500-mil centers, as shown in the enlarged photo above.

Here are some of the major benefits of our fine-line circuits:

- *Broad design flexibility* allowing ground plane placement next to dense, fine-line traces.
- *Superior electrical performance* for high speed controlled impedance circuits and minimized EMI, due to uniform and predictable fine-line conductor geometries.



Note the superior side-wall characteristics of the 6-mil trace.

- *Improved assembly yields and long-term field reliability* assured by superior solder mask coverage and uniform thickness over bare copper circuitry.

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- *Transducers: 1-6V*
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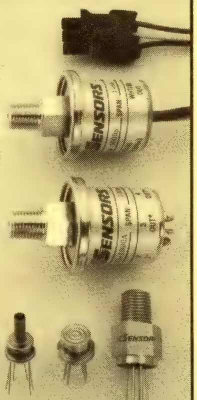

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OC8000

EXPANDS PC PERFORMANCE AT A FRACTION OF NETWORKING COST

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STAR GATE

CIRCLE NO 198

A high quality video camera you can plug in and forget!

Here is a new one-piece camera designed for long-term unattended operation in machine vision, instrumentation and medical systems. Called the "Visioneer," this new camera is extremely temperature stable. When required, maintenance couldn't be simpler. All boards are plug-in modules, and all board level maintenance can be done with just a screwdriver. Bandwidths are available up to 25 MHz, with line rates from 525 to 1023. Camera includes external drive and internal sync generator for automatic backup. If you have special requirements, ask us to customize this camera. It's designed for that, too. From the company with 20 years experience in designing video cameras of the highest quality.

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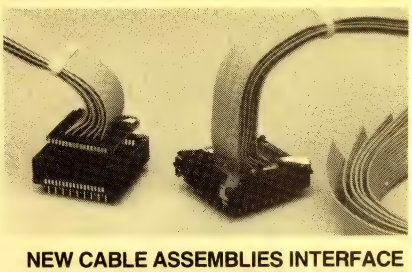
CIRCLE NO 199



NEW CABLE ASSEMBLIES INTERFACE 68-PIN JEDEC CHIP CARRIER SOCKETS TO EMULATORS AND TEST EQUIPMENT

Series CA-1623 chip carrier socket-to-emulator interface cables are for both leaded and leadless 68-pin JEDEC chip carriers. Establish remote access to all contact positions for test and emulator functions. Interface plug included. Mounts in all chip carrier sockets. Its cable is 24" long with cut-wire termination. Wire size 28 or 30 AWG with .050" center leads.

METHODE ELECTRONICS, INC.
INTERCONNECT PRODUCTS DIVISION
1700 Hicks Road, Rolling Meadows, Illinois 60008
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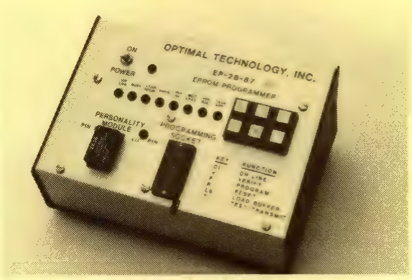

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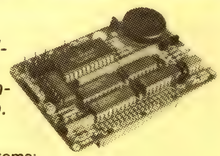

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Multibus, Multimodule TM Intel Corp.

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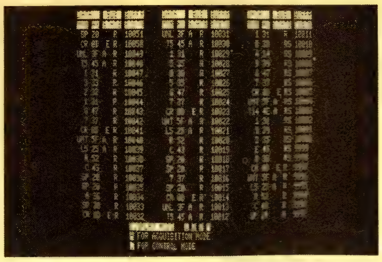

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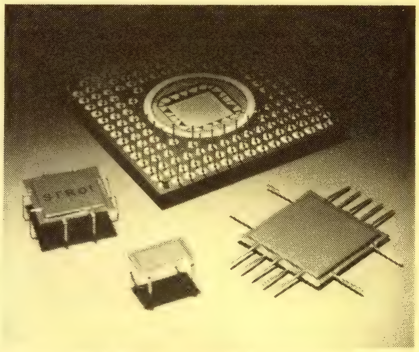

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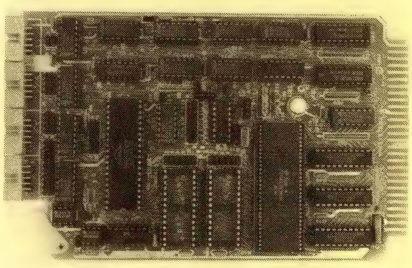

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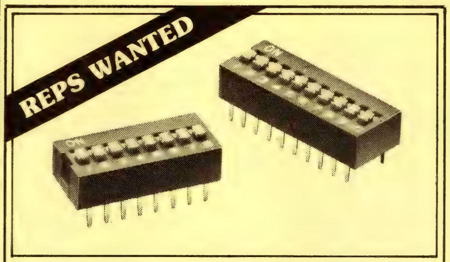

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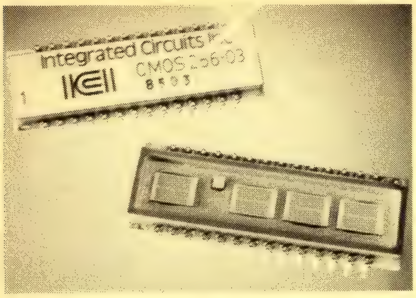

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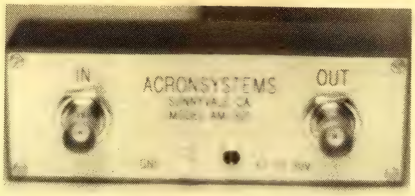

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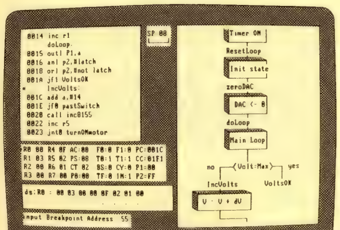

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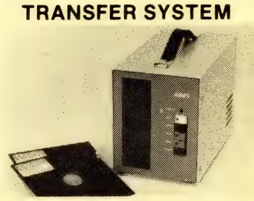

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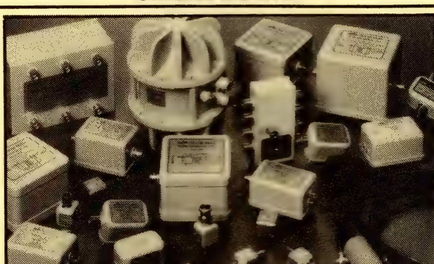

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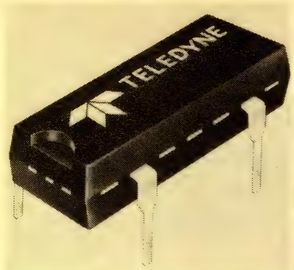

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Teledyne's 641 AC relay provides a triac output rated at 1/2 amp up to 50°C ambient without a heat sink. Transformer isolation is 2500VRMS, turn-on time is 2μsec. Other features include TTL compatible input, 10 amp surge capability, low minimum output current (5mA), UL recognized, CSA certified. Hybrid microcircuit assembly is molded in a TO-116 plastic DIP. Model 643 is the DC version. Priced in quantity at $6.55 ea.

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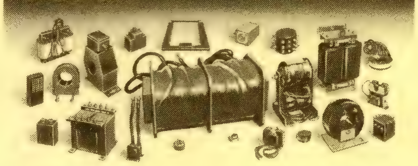

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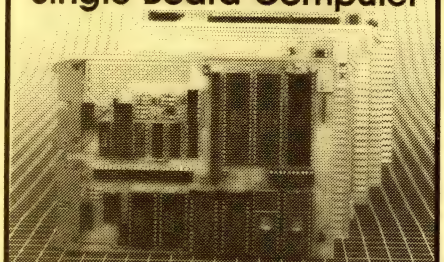

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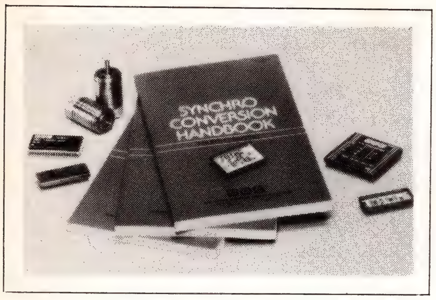

Revised handbook covers synchro-conversion topics

The 116-pg revised edition of the *Synchro Conversion Handbook* includes a new section that lists application notes and another new section that serves as a guide to the manufacturer's products. The handbook covers such topics as the fundamentals of angle-sensing transducers and data-conversion devices, theory of operation, measuring and computing performance parameters, and design constraints and selection criteria. The handbook acquaints you with the principles of synchro conversion and provides insights into the tradeoffs between different methods.

ILC Data Device Corp, Marketing Dept, 105 Wilbur Pl, Bohemia, NY 11716.

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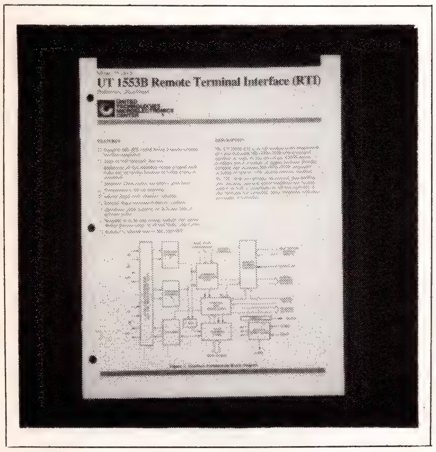

MIL-STD-1553 interface explored

This preliminary data sheet covers the manufacturer's MIL-STD-1553B remote-terminal interface, the UTI 1553B RTI. Through text, tables, and diagrams, the 20-pg publication covers interface features, electrical characteristics, the interface architecture, and a pinout description. It also includes sections on general information, transparent memory access, and the control register. In addition, it provides timing diagrams and outline diagrams. The pamphlet is 3-hole punched for loose-leaf filing.

United Technologies Microelectronics Ctr, 1575 Garden of the Gods Rd, Colorado Springs, CO 80907.

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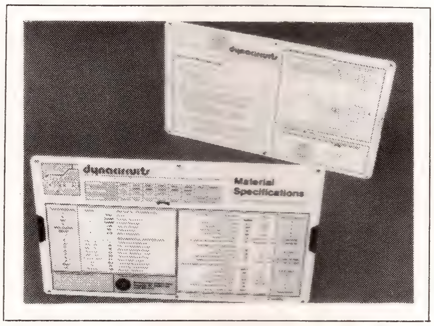


Chart gives material specs

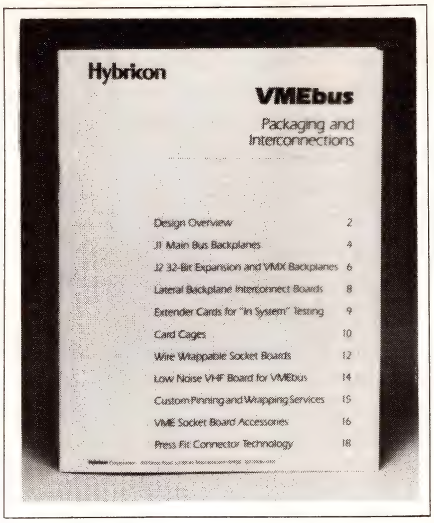
This slide chart features material specifications for pc boards. The chart offers at-a-glance information on physical, mechanical, electrical, and thermal properties of different grades of materials from different manufacturers. Also covered are tooling concepts and the use of raw materials. Send business card with your request.

Dynacircuits Inc, 11230 Addison St, Franklin Park, IL 60131.

INQUIRE DIRECT

VME Bus packaging highlighted

VMEbus Packaging and Interconnections is a 20-pg book that helps you advance VME Bus systems from logic and circuit design to the finished product. The book begins with an overview of VME Bus characteristics, features, and standards, and goes on to explain interconnection and packaging considerations and alternatives in terms of system performance. The book includes



specs for card cages, backplanes, VME interconnect boards, and wire-wrapped circuit boards, as well as test-extender cards and accessories. Also covered are the manufacturer's engineering and manufacturing support services.

Hybricon Corp, 410 Great Rd, Littleton, MA 01460.

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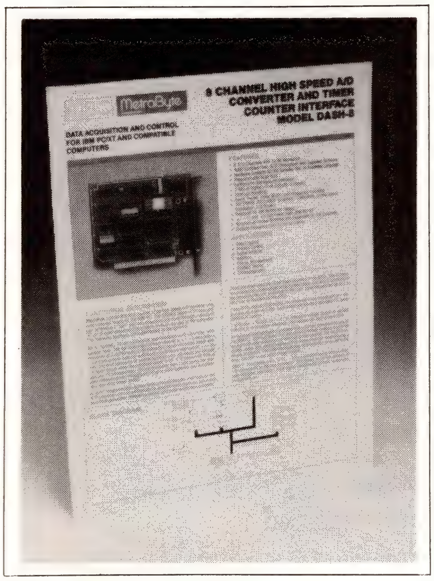

Data sheet probes A/D converter and counter/timer

Describing the Dash-8 A/D converter and counter/timer board, this data sheet probes input resolution, accuracy, and sample rates as well as temperature coefficients and drift rates. The sheet also details the software provided with the Dash-8, which suits the IBM PC, PC/XT, PC/AT, and compatible computers. In addition, it describes the board's counter/timer capabilities, digital-I/O functions, and accessory boards.

MetraByte Corp, 254 Tosca Dr, Stoughton, MA 02072.

Circle No 408

High-reliability custom hybrids covered

Custom Hybrids for Space and Hi-Rel: Survival of the Fittest is a 4-color brochure that describes the company's Class S and B custom-hybrid manufacturing capability. The hybrids use thick- and thin-film technologies to package circuits from dc to 22 GHz.

Frequency Electronics Inc, 55 Charles Lindbergh Blvd, Mitchel Field, NY 11553.

Circle No 409

Microwave parts described

The manufacturer's line of microwave components, including coaxial and waveguide switches, dummy loads, and crystal detectors, are detailed in this 24-pg brochure. Also presented are bolometers and RF micropotentiometers. Among the coaxial switches described are high-frequency, high-power devices that spec 1M-cycle reliability. The company supplies waveguide switches for L band to KU band and three

series of dummy loads (medium-power, high-power, and liquid-cooled), as well as 50W coaxial miniature dummy loads.

Micronetics Inc, 36 Oak St, Norwood, NJ 07648.

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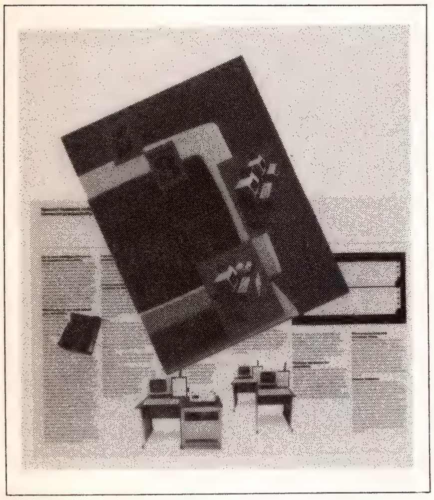

Brochure highlights communications terminal

A multiport, multifunction message-communications terminal is the subject of this 6-pg, 4-color brochure. The publication describes capabilities and specs for the enhanced Micronet 8, which can now have as many as nine configurable ports. The unit lets you combine Telex, high-speed, leased, and other telecommunications lines.

Sidereal Corp, 9600 SW Barnes Rd, Portland, OR 97225.

Circle No 411

IR products characterized

Through diagrams, charts, and illustrations, this comprehensive data book characterizes approximately 400 IR-emitting products. The 448-pg document covers IR diodes, photosensors, and optically coupled isolators. It also details slotted optical switches, reflective sensors, and Hall-effect switches. The publication includes a device index, a product-selection guide, and a glossary. In addition, application notes describe methods and techniques for using the devices.

TRW Electronic Components Group, Optoelectronics Div, 1207 Tappan Circle, Carrollton, TX 75006.

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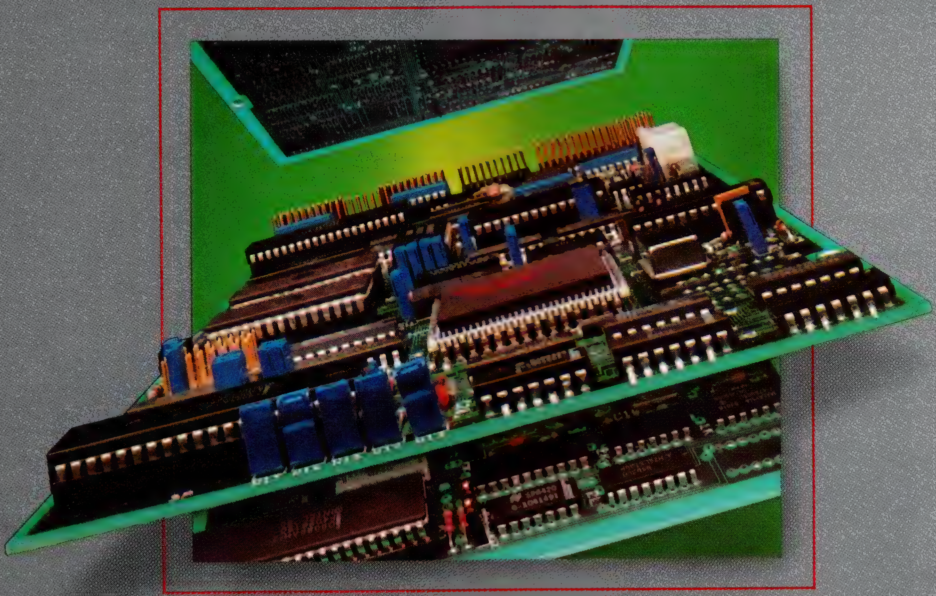

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CIRCLE NO 158

Starting a business in an incubator gives entrepreneurs the edge on success

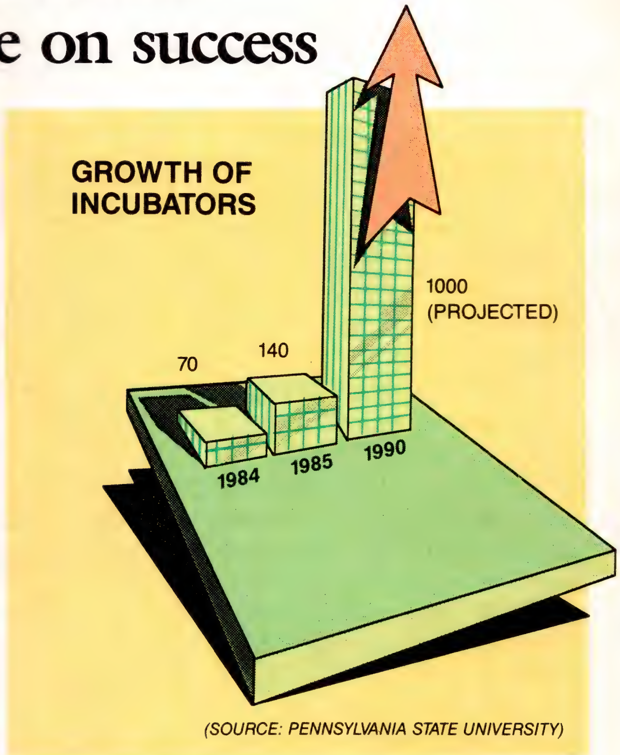
Deborah Asbrand, *Staff Editor*

Small-business entrepreneurs are finding inspiration in the maxim that there is strength in numbers, and they're putting it to use in a way that gives their young companies added chances for success. Instead of single-handedly taking on the financial burdens of setting up new businesses, entrepreneurs are taking advantage of business incubators, which allow new companies to share work space and operating expenses while they make their way through the start-up stage.

Incubator tenants share telephone and secretarial services, word-processing and photocopying equipment, conference rooms, and sometimes access to computer terminals. Perhaps of greater importance than the shared support services is the readily available assistance of financial, marketing, and accounting consultants. After a period of two to three years, the businesses are ready, and in most cases required, to move out of the facility and begin operating independently.

Incubators' supportive environments are particularly attractive to high-technology and electronics companies, which often go without sales income through the long periods of initial product development. For the technical specialist at the helm of an electronics company, the consulting services can be a boon. "For many engineers, incubators can bring business and financial sense to their business," says University of Minnesota researcher Candace Campbell.

Incubators first emerged in the mid-1970s when a number of urban communities hit upon the idea as a means of starting new businesses to stimulate local economies and to provide jobs. Since 1983, the concept has rapidly caught on throughout the public and private sectors and even at universities. Pennsylvania State University researcher David Allen identified 70 incubators in operation in December 1984; one year later, that number had nearly doubled. Allen predicts that 1000 incubators will be in operation by 1990.



Lending credence to Allen's optimistic forecast are the 10,000 inquiries about incubator programs that flooded the US Small Business Administration's Office of Private Sector Initiatives during a recent 12-month period. The Office of Private Sector Initiatives held seven conferences on incubators last year. These conferences were attended by more than 2500 people.

Response to economic realities

Shifting economic factors are primarily responsible for the rapid growth and acceptance of the incubator concept. Many cities that relied heavily on such traditional industries as steel, automobiles, or textiles had their economic security pulled out from beneath them when these industries foundered and closed factories. Faced with staggering unemployment and dim prospects for attracting large industrial tenants to occupy the vacated buildings, communities were forced to look for innovative ways to use the space and create new jobs.

To accomplish these goals, communities collaborated with the private sector in ways that benefited both parties. For example, when Olin Corp announced plans to vacate the 80-acre industrial site it occupied in New Haven, CT, city officials were left with the problem of what to do with the site's 20 buildings and more than 3 million square feet of space. Olin donated the buildings to the city, thus earning a tax write-off and the city's goodwill. Funding from the city, the state, Yale University, and Olin laid the groundwork for the Science Park Development Corp, a business rehabilitation and development project that now includes two incubator facilities. These incubators house 75 small businesses.

While the nation's changing economic landscape posed problems for city and state communities, the attempt to solve those problems threw a new light on the economic contributions of small businesses. It became clear that cultivating small businesses made sense: Small companies employ 48% of the nation's workers and generate 38% of the gross national product. At the same time that local governments and private concerns were discovering the potential of small businesses to bolster local economies, increasing numbers of workers were finding the idea of starting a new business irresistible. In 1984, 102,329 small companies opened their doors, up 16% from 1979.

Nurturing the growth of these young companies, and thereby increasing their chances of survival so that they might expand and become profitable, was a sensible, yet unexplored, option. Bringing the businesses together to share space and support services was seen as a way to boost their chances of success and provide safe passage through the critical first years of operation. Indeed, start-up companies can use all the support they can get: The Small Business Administration estimates that 70% of small businesses fail within the first five years.

Incubators differ in methods

"No two incubator facilities are exactly alike," says Campbell. "Each has been developed to meet its own market niche." Private concerns have different reasons for providing the service than city and state governments, and even within the private sector the rationale can vary. An example of private-sector involvement in incubators is Control Data Corp, which opened its first Business and Technology Center in 1979 near the company's headquarters in the Minneapolis-St Paul area. The company now owns or licenses 24 incubator facilities with more than 700 tenants. Businesses started in the Business and Technology Centers have generated more than 6000 jobs in the last six years.

Tenants in Control Data's centers have access to a telephone-answering service, word processors, and photocopiers. The centers also provide discounts on equipment, car rentals, and group health and life insurance plans. Consultants are available on a contractual basis. In addition, the businesses are electronically linked through a network that allows them to list their products, prices, and services. A database provides information about government contracts.

"For many engineers, incubators can bring business and financial sense to their business."

What Control Data gains from its centers is a ready market for its computer-based education and training programs for small-business managers. The company hopes that, once a business leaves the incubator, it will continue to use Control Data's training programs as well as its accounting and spreadsheet software packages.

The Rubicon Group in Austin, TX, is a different kind of privately sponsored incubator. Tenants who set up shop in the facility pay for neither the work space they use nor the support and consulting services that the Rubicon Group's staff of 35 provides. Instead, the Rubicon Group takes a 25 to 75% stake in each business. The facility's tenants are all hardware, software, or systems companies. By giving each start-up careful attention, founder Steve Szygenda, a former engineer, is banking on producing successful, profitable ventures.

Szygenda has been surprised and pleased that many of his incubator's applicants have been older—and therefore more experienced—technical professionals. "We're finding people with 20 years' experience who want to take a crack at their own business, which is even better because they know their industries," he says.

Screening processes vary

The screening process for applicants varies at each incubator. Some facilities are open to any entrepreneur as long as space is available. Others, like the Rubicon Group, are looking for technology-based companies that have better-than-average chances of earning a high return on investment. At the Advanced Technology Development Center (ATDC) in Atlanta, GA, applicants go through a rigorous process of developing a business plan that must then be presented to and approved by a review panel.

ATDC is part of the University System of Georgia and is governed by its board of regents. Its tenants maintain strong ties to the university system and have access to university laboratories, equipment, and library services. Tenants are "essentially taken into the university community with us as their spon-

For more information . . .

More information on incubators is available from the US Small Business Administration, Office of Private Sector Initiatives, 1441 L St NW, Washington, DC 20416; phone (202) 652-7880. The office publishes a monthly newsletter, *Incubator Times*, that contains general information and conference dates and cites other sources of information on incubators. The newsletter is free upon request.

sor," says Don Plummer, manager for research and communications at ATDC.

"If you don't need the services of the university or don't benefit from the shared services, we'll probably recommend you locate somewhere else and use our consulting services," says Plummer. "We try to reserve this space for people who need contact with the academic community."

The center has come a long way from its beginning in 1980 in a renovated high school. It now occupies 83,000 square feet in two new buildings constructed at a cost of $6.1 million. The buildings house 20 tenants and offer office, laboratory, and light manufacturing space. The success record of ATDC's new businesses is admirable: Of the 40 companies that have moved out of the incubators, only eight have failed.

Chances for success improve

The ATDC success rate is indicative of the fortunes incubators can bestow. The chances of success for those businesses that spin out of incubators are higher than for those companies that begin operations independently. Allen's reseach shows that two-thirds of the companies that spend their early years in an incubator survive.

For business owners, the most important part of starting out in an incubator isn't just the shared services. Neighboring entrepreneurs, who are encountering the same obstacles or have met the same problems and can offer advice on how to solve them, become ready-made colleagues. Many incubators regularly hold round-table sessions that give business owners and managers opportunities to talk about their frustrations and their successes. **EDN**

Section Interest Quotient
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CAREER OPPORTUNITIES

1986 Editorial Calendar and Planning Guide

Issue Date	Recruitment Deadline	EDN Editorial Emphasis	EDN CareerNews
Mar.6	Feb. 7	Semicustom IC (Array) Directory (CAE-related*); Communications ICs; Computer Board Directory; Connectors	Closing: 3/13 Mailing: 3/25
Mar. 20	Feb.21	Test & Measurement; Analog ICs; Computer Peripherals; Support Chip Directory	
Apr. 3	Mar. 7	Communications Special Issue; Communications ICs; CAE; Buses; April Fools Supplement	Closing: 4/10 Mailing: 4/22
Apr. 17	Mar. 21	Power Supplies; Development Software; Memory Technology; Computer Graphics Devices (CAE-related*); Electro '86 Product Preview	
May 1	Apr. 4	Electro '86 Show Issue; Sensors/Transducers; ICs; Test & Measurement; Display Technology	Closing: 5/8 Mailing: 5/20
May 15	Apr. 18	Programmable Logic Devices; CAE; Communications Components; Optoelectronics	
May 29	May 2	Analog Technology Special Issue; Data Converters; Analog ICs	

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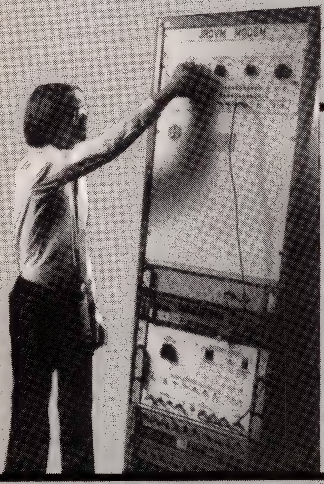

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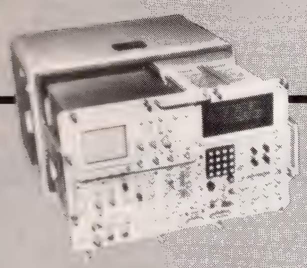

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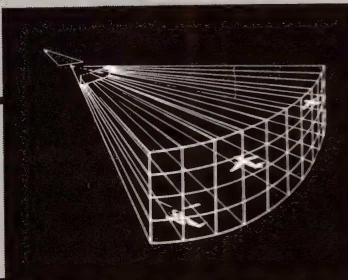

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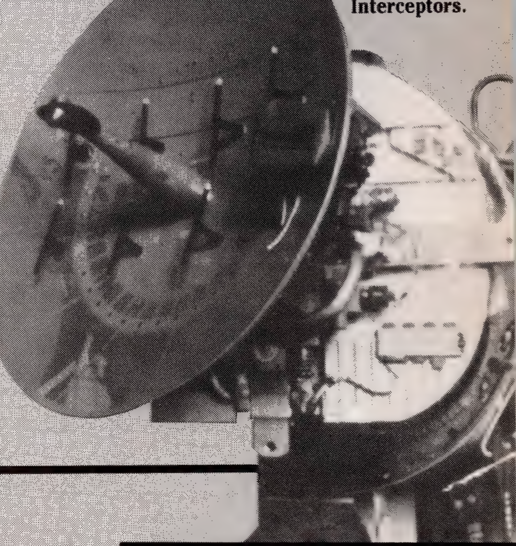

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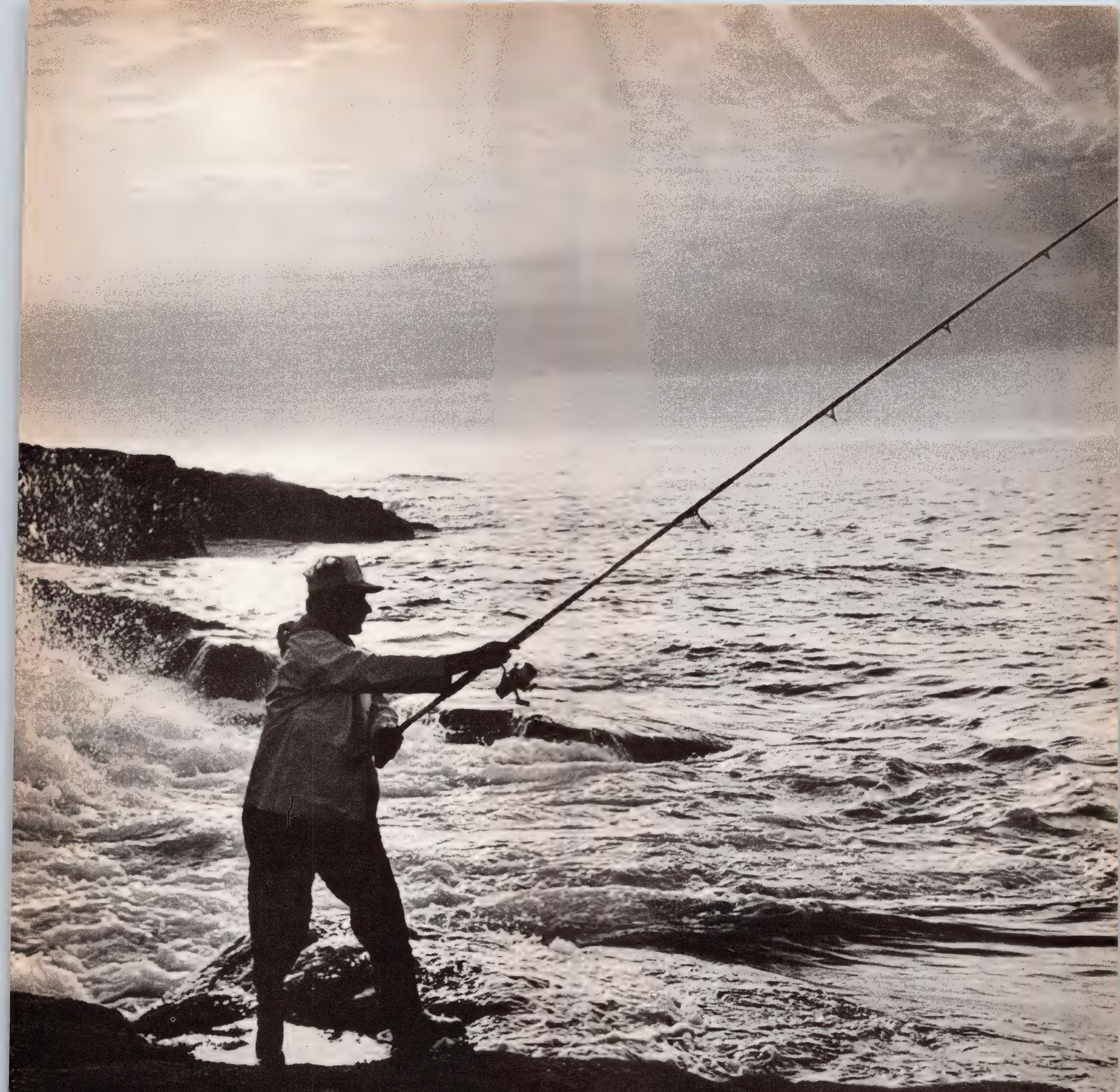

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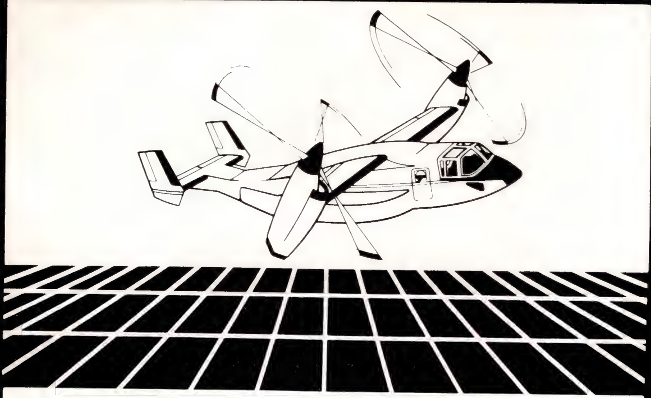

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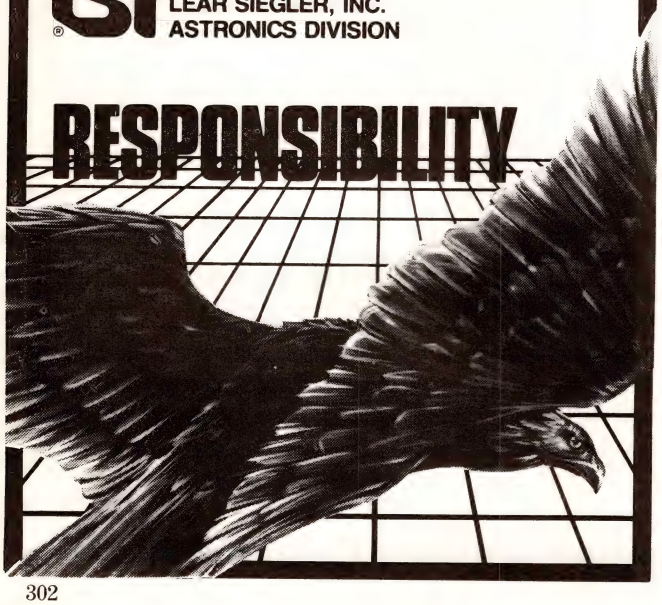

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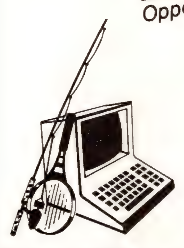

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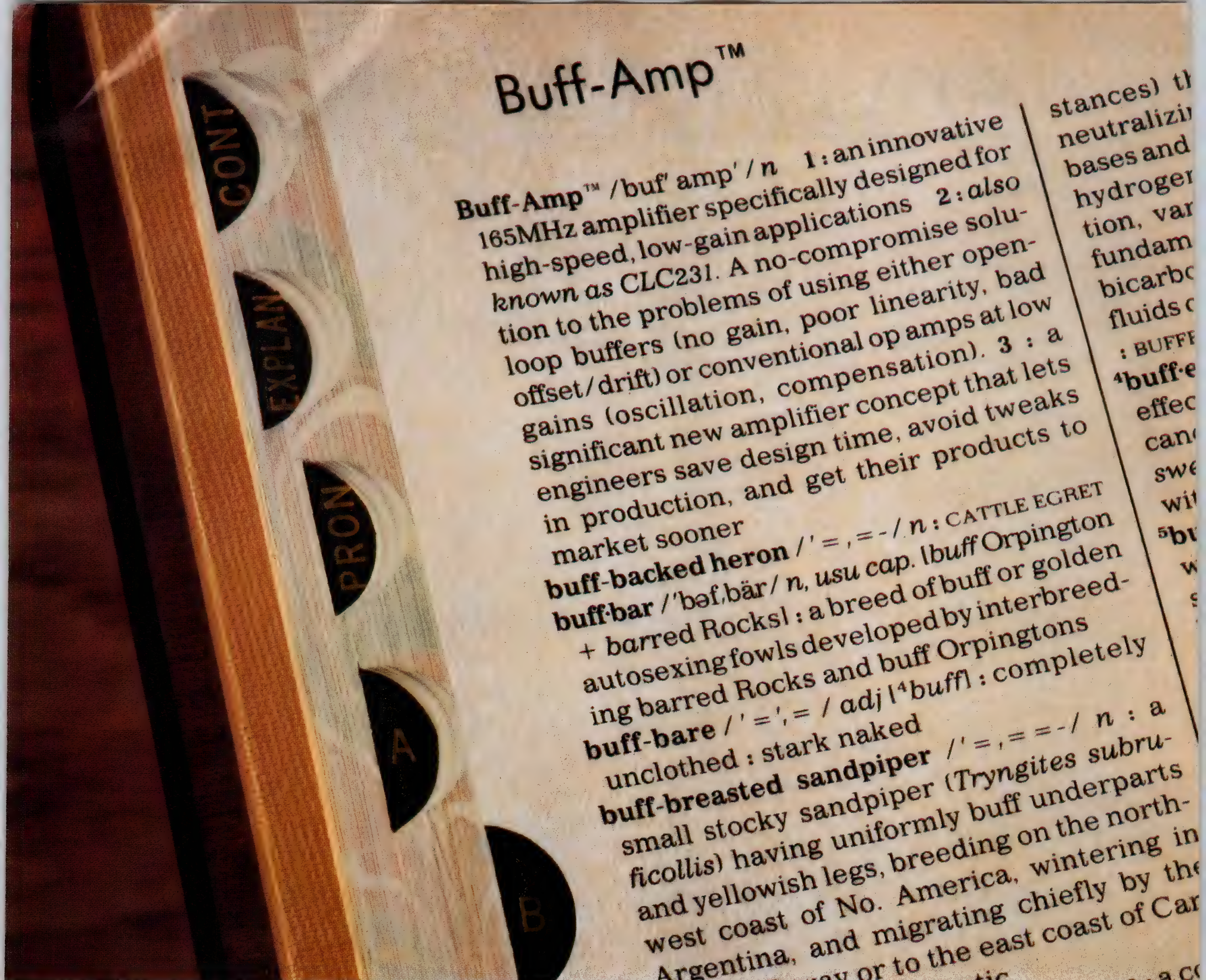

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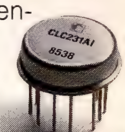


Comlinear Corporation

CIRCLE NO 159

EDITED BY GEORGE STUBBS

Growth in LAN use is key to improved plant productivity

Managers in the US manufacturing community are increasingly looking to local-area networks as essential elements of the attempt to improve manufacturing productivity and the quality of products. According to Venture Development Corp, the full benefits of automation can only be realized when automated processes are integrated and all manufacturing information can be shared. With this in mind, 50% of respondents to a VDC survey indicated that they plan to install LANs in their manufacturing facilities by 1990.

Almost three-quarters of the respondents prefer an industry standard in plant communication systems. They noted that, though integration is necessary, current communication methods are expensive, and additional costs are incurred when new systems are installed and rendered compatible with the existing communication system. Custom hardware and software interfaces, introduced by vendors interested in establishing their own proprietary communication techniques, are also costly. Communication standards would help hold down the costs of plant integration.

The majority of LANs installed to date transmit data at speeds of less than 2M bps, says VDC. Respondents to the survey indicate, however, that higher transmission speeds—perhaps even to 20M bps—will definitely be needed. Users currently connect approximately 50 to 100 devices in their networks. The required number of network nodes should increase over the next five years.

Respondents also reported that their technology and architecture choices will change. Currently, users prefer to connect nodes via proven coaxial cable, but they expect fiber-optic systems to overcome their current technological limitations. Fiber-optic systems will readily handle the broad system bandwidths that future LANs hope to attain. Also, today's networks—particularly those that manage some subset of a plant's operation—typically use a bus structure. Future networks will integrate plant operations by connecting several buses, or subnetworks, in a grid-like architecture.

USER PREFERENCES FOR FEATURES OF AN INDUSTRIAL LOCAL-AREA NETWORK

NETWORK FEATURE	PLANTWIDE NETWORK NOW	PLANTWIDE NETWORK FUTURE	SUBNETWORK NOW	SUBNETWORK FUTURE
TOPOLOGY	BUS	BUS	BUS	BUS
BANDWIDTH	BROADBAND	BROADBAND	BASEBAND	BASEBAND
CABLE TYPE	COAXIAL	FIBER OPTIC	COAXIAL	FIBER OPTIC
SPEED	10M BPS	20M BPS OR HIGHER	5M BPS	10M BPS OR HIGHER
NUMBER OF NODES	50 TO 100	100 TO 200	LESS THAN 20	20 TO 50
TYPICAL DISTANCE	1 TO 3 MILES	1 TO 3 MILES	½ MILE	½ TO 1 MILE

(SOURCE: VENTURE DEVELOPMENT CORP.)

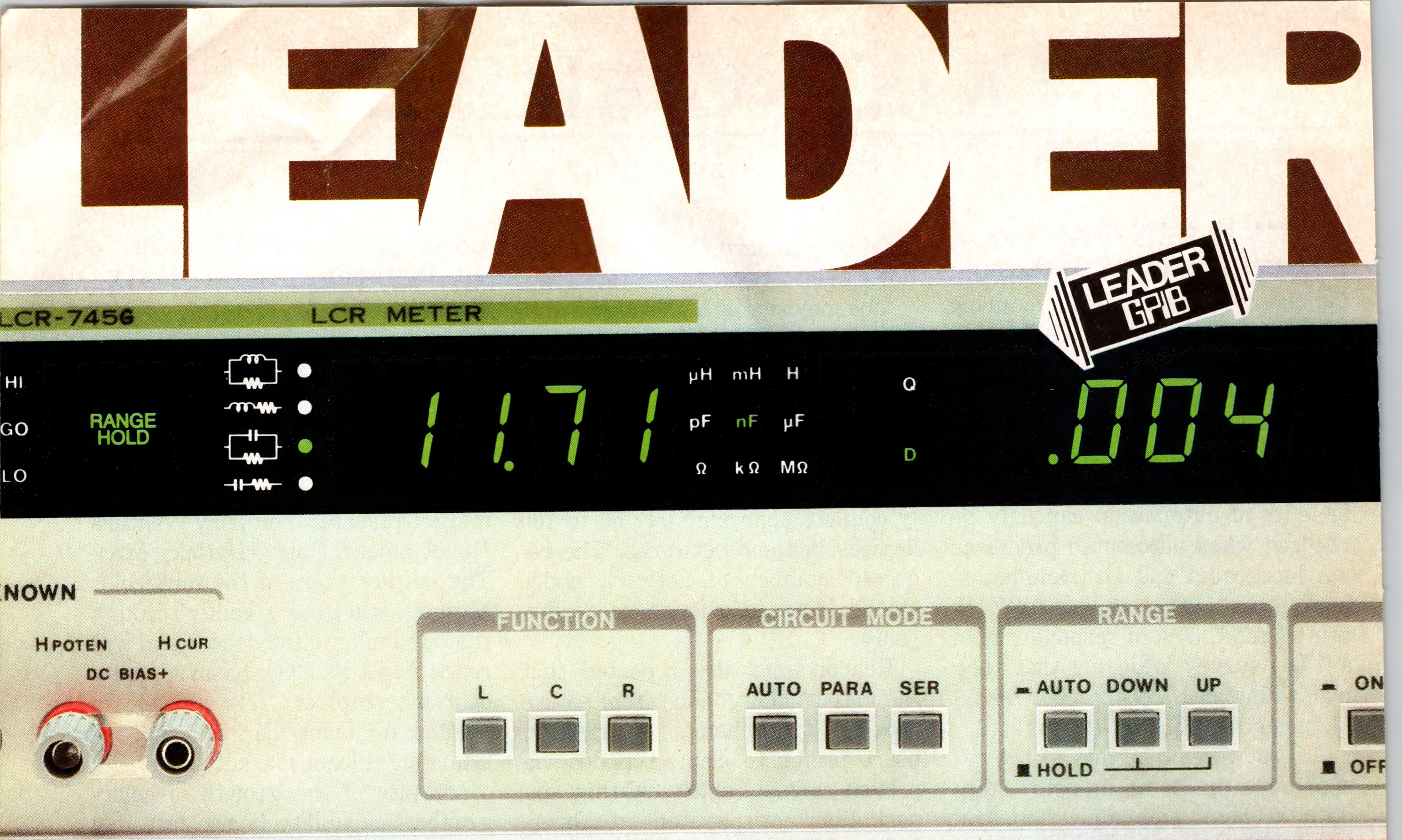
Color-graphics CRTs gain on monochrome, but slowly

In the market for raster-scan CRT graphics terminals, the improving resolutions and falling prices of color-graphics units are giving them the edge in user demand. In 1984, 61.4% of all graphics CRTs shipped were multicolor devices, reports the market-research company Venture Development Corp (Natick, MA). The market share of the multicolor segment will grow steadily through the remainder of the decade and will reach 79.5% by 1990. Even so, monochrome-graphics CRTs will remain popular for many uses and will retain a significant market share.

In spite of the growth of color-graphics capability in the last five years, monochrome-graphics CRTs are still in widespread use in installations with large numbers of terminals. In such installations, a central multicolor terminal or a color-output peripheral serves users' needs for multicolor display. Monochrome graphics are popular in previewing applications, where the use of color is not normally justified. In addition, for many scientific and technical applications monochrome displays are sufficient to provide the information needed. Many graphs and high-resolution plots, quick scans of data, and strictly numerical results don't exercise the full potential of multicolor CRTs.

The fastest growing application for monochrome-graphics CRTs will be in education; the number of monochrome terminals in such environments will grow at a 25% rate, from 6800 installed units in 1984 to 26,400 installed units by 1990. Use of monochrome CRTs will also grow rapidly in simulation and process control.

Process control is also a popular application area—the most popular, in fact—for color-graphics CRTs. Business graphics, CAD/CAM, and other engineering applications will also help sustain the growth in use of multicolor graphics terminals.



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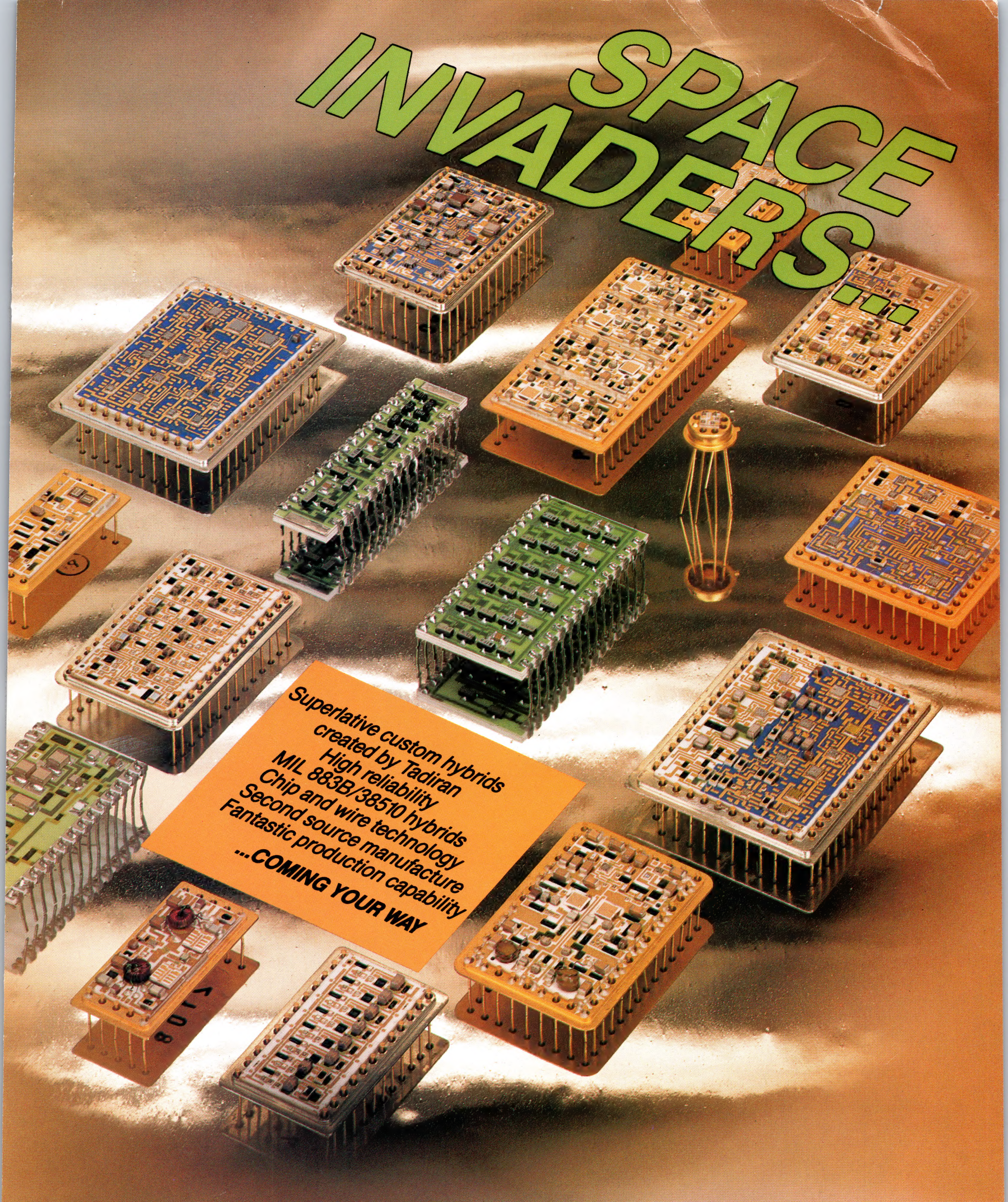
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